ES1988 Allegro™
PCI Audio-Modem Accelerator
Data Sheet

ESS Technology, Inc.

DESCRIPTION

The ES1988 Allegro™ PCI audio-modem accelerator combines advanced audio and modem functionality in a highly integrated PCI solution. Utilizing one PCI load, the ES1988 provides a two chip audio-modem solution with digital interface capability to an AC'97 CODEC in the dock (a.k.a. digital docking). The ES1988 is designed to provide a low cost, high-performance solution for notebook PC applications.

The high-bandwidth PCI bus and an integrated high-fidelity CODEC are utilized to deliver advanced PC audio features, such as DirectSound acceleration, and HRTF 3-D positional audio. The ES1988 implements multi-stream DirectSound and DirectSound3D acceleration with digital mixing, sample rate conversion and HRF 3-D filtering for two speaker 3D positional audio.

The programmable audio signal processor provides support for multiple audio streams. With its built-in DSP core, the ES1988 uses its dedicated DMA engine to handle complex signal processing tasks with a bus-mastering PCI interface. The support functions ensure efficient transfer of audio data streams to and from system memory buffers, providing a system solution with maximum performance and minimal host CPU loading. The architecture enables implementation of communications over the Internet from multiple sources.

The ES1988 maintains full DOS legacy audio compatibility over the standard PCI 2.1 and PCI 2.2 bus. Full DOS game compatibility is ensured through either PC/PCI, Distributed DMA (DDMA), or Transparent DMA (TDMA).

The ES1988 includes an HSP modem interface via its secondary AC-Link connecting with the ES2828 MC'97 CODEC. The MC'97 is used as the analog front end for the modem and DAA control. The ES56 V.90 data/fax/TAM modem runs on the host while the ES1988 serves as the bi-directional buffer for data transmission and reception. The modem functions include the standard AT command set, V.42*bis* and Group 3 Fax.

The ES1988 provides a high-quality docking solution through proven AC-link based digital docking. This is accomplished using only a five wire digital connection. The secondary AC'97 link (extension 2.1 compliant) of the ES1988 interfaces to a secondary AC'97 CODEC in the dock to provide high quality audio in the dock.

The ES1988, which operates at 3.3 volts digitally and 5.0 volts in analog, is compliant with the Advanced Power Management (APM) 1.2, Advanced Configuration and Power Interface (ACPI) 1.0, and PCI Power Management Interface (PPMI) 1.0. The ES1988 supports D0, D1, D2, and D3 (hot and cold) power-saving modes for power efficiency when the audio system is both active and idle. CLKRUN# support is also available.

The ES1988 is available in an industry-standard 100-pin Thin Quad Flat Pack (TQFP) package.

AUDIO FEATURES

- High-performance single-chip PCI audio acceleration
- Integrated high-fidelity AC'97 codec
- Multi-stream DirectSound and DirectSound 3D acceleration
- Sensaura CRL Positional 3D
- High-quality sample rate conversion and digital mixing
- Direct Music support
- Realtime effects processing
- S/PDIF output for PCM or AC-3 content
- Full legacy DOS game support using TDMA, PC/PCI or DDMA hardware implementation methods
- Supports one additional PCI bus master devices
- HSP modem interface via MC'97 link
- Supports wakeup-on-ring
- Digital docking via secondary AC-Link

MODEM FEATURES

- Data Mode capabilities:
  - V.90 56K bps
  - V.34 33.6 kbps and fallbacks
  - Standard AT command set
  - V.42 (LAPM) and MNP error correction
  - V.42bis/MNP 5 data compression
  - 3.3 V power supply with 5V-tolerant inputs
- Fax Mode capabilities:
  - ITU-T V.17, V.21 ch2, V.27ter, V.29
  - Group 3 (TIA/EIA 578 Class 1 and Class 2)
- Supports Wakeup On Ring from D3$_{hot}$ and D3$_{cold}$ states and DAA control

POWER MANAGEMENT

- Compliance with APM 1.2, ACPI 1.0, and PPMI 1.1
- Compliance with Intel's "Mobile Power Guidelines '99"
- 3.3 volt digital operation with 5V-tolerant inputs
- 5.0 volt analog operation

COMPATIBILITY

- Supports PC DOS games and applications for Sound Blaster and Sound Blaster Pro
- Supports Microsoft® Windows™ SoundSystem™
- Meets PC99 and WHQL specifications
- Compliant with Intel's Audio/Modem Riser Card and mini-PCI specifications

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FIGURES

TABLES

PINOUT

Figure 1 ES1988 Allegro Pinout

PIN DESCRIPTION

Name	Number	I/O	Description
C/BE[3:0]#	1, 13, 20, 30	I/O	PCI command/byte enable. During address phase of a transaction, these pins define the bus command. During data phase, these pins define the byte enable.
IDSEL		I	ID Select. When pin 2 is configured as a multifunction pin (see pin 2 note), IDSEL is selected internally to AD24.
R0#		I	PCI bus request 0 input from external PCI master device. RO# is enabled by setting the PCIx2 arbiter bit PCI 58h [0] = 1. Select RO# from pin 2 by setting PCI 58h [10] = 1, and pin 2 must be configured as a multifunction pin (see pin 2 note). Either pin 2 or pin 52 may be used for R0#.
SPDIFO	2	O	S/PDIF Output. Enable SPDIFO by setting PCI 53h [0] = 1. Select SPDIFO from pin 2 by setting PCI 58h [1] = 1, and pin 2 must be configured as a multifunction pin (see pin 2 note). Either pin 2 or pin 54 may be used for SPDIFO.
PCREQ#		O	PC/PCI request output. Enable PCREQ# by setting PCI 50h [10:8] = 010. Pin 53 is used as PCREQ# when configured as an audio-only device. PCREQ# can only be used from pin 2 when the ES1988 is configured as a multifunction device (see pin 60 note). Pin 2 must be configured as a multifunction pin (see pin 2 note).
(note)			Pin 2 is configured as a multifunction pin when pin 85 is pulled low. This will allow for additional use of this pin for RO#, SPDIFO, or PCREQ#. If pin 85 is open or pulled high, then pin 2 may only be used as IDSEL.
GND	3, 21, 40, 89	I	Digital ground
AD[31:0]	93:100, 4:11, 22:29, 31:38	I/O	Address and data lines from the PCI bus
VCC	12, 41, 90	I	Digital supply voltage, 3.3V
FRAME#	14	I/O	Cycle frame
IRDY#	15	I/O	Initiator ready
TRDY#	16	I/O	Target ready
DEVSEL#	17	I/O	Device select
STOP#	18	I/O	Stop transaction
PAR	19	I/O	Parity
CLKRUN#	39	I/O	CLKRUN#, is I/O pin for PCI Clock status and an output to start or accelerate clock function by enabling PCI 52h [11] = 1.
ECS		O	Chip select output to EEPROM chip select input. ECS is active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
GD[0]	42	I/O	Game port data Input/Output
GD[1]	43	I/O	Game port data Input/Output
EDOUT		O	Data output to EEPROM data input. EDOUT goes active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
GD[2]		I/O	Game port data Input/Output
EDIN	44	I	Data input from EEPROM data output. EDIN goes active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
VOLUP#		I	Hardware volume control (volume up). Used in combination with pin 45 (VOLDN#). Hardware volume control is enabled by setting PCI 52 [7] = 1. Pins 44:45 is selected for hardware volume control by setting PCI 52h [5] = 1. Pins 53:54 may also be used for hardware volume control.

Name	Number	I/O	Description
GD[3]		I/O	Game port data Input/Output
ECLK		O	Clock output to EEPROM clock input. ECLK goes active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
VOLDN#	45	I	Hardware volume control (volume down). Used in combination with pin 44 (VOLUP#). Hardware volume control is enabled by setting PCI 52 [7] = 1. Pins 44:45 is selected for hardware volume control by setting PCI 52h [5] = 1. Pins 53:54 may also be used for hardware volume control.
GD[4]	46	I	Game port data input
GD[5:7]	47:49	I	Game port data input
GPIO[13:15]		I/O	General purpose input/output
I2SCLK		I	I^{2}S serial clock input. I^{2}S input is enabled by setting Allegro_Base+37h [15] = 1.
SIRQ#	50	I/O	Serial interrupt request. Optional PC/PCI system implementation. Serial IRQ is enabled by setting PCI 40h [14] = 1.
GPIO4		I/O	General purpose input/output
I2SLR		I	I^{2}S frame sync input. I^{2}S input is enabled by setting Allegro_Base+37h [15] = 1.
GTO#		O	Grant to PCI master. GTO# is enabled by setting PCIx2 arbiter bits PCI 58h [0] = 1 and PCI 58h [11] = 1. Select GT0#/GSO from pin 51 by enabling PCI 58h [10] = 0. Pin 63 may also be used as GT0#/GSO.
GSO	51	O	Grant select 0 output to control external quick switch to grant PCI master phase. GSO is enabled by setting PCIx2 arbiter bit PCI 58h [0] = 1 and PCI 58h [11] = 0. Select GS0/GT0# from pin 51 by enabling PCI 58h [10] = 0. Pin 63 may also be used as GT0#/GSO.
GPIO5		I/O	General purpose input/output
I2SDATA		I	I^{2}S data input. I^{2}S input is enabled by setting Allegro_Base+37h [15] = 1.
R0#	52	I	PCI bus request 0 input from external PCI master device. RO# is enabled by setting the PCIx2 arbiter bit PCI 58h [0] = 1. Select R0# from pin 52 by enabling PCI 58h [10] = 0. Either pin 2 or pin 52 may be used for R0#.
GPIO6		I/O	General purpose input/output
MC_97DI		I	Modem CODEC data input. Enabled by setting Allegro_Base+38h [3] = 1.
PCREQ#		O	PC/PCI request output. Enable PCREQ# by setting PCI 50h [10:8] = 010. Pin 53 is used as PCREQ# when configured as an audio-only device. PCREQ# can only be used from pin 2 when configured as a multifunction device (see pin 60 note).
VOLUP#	53	I	Hardware volume control (volume up). Used in combination with pin 54 (VOLDN#). Hardware volume control is enabled by setting PCI 52 [7] = 1. Pins 53:54 is selected for hardware volume control by setting PCI 52h [5] = 0. Pins 44:45 may also be used for hardware volume control.
GPIO7		I/O	General purpose input/output

Name	Number	I/O	Description
PME#		O	PME# output to wake up the system. PME is enabled by setting the PME_EN bit (PCI C5h [0] = 1).
SPDIFO		O	S/PDIF Output. Enable SPDIFO by setting PCI 53h [0] = 1. Select SPDIFO from pin 54 by setting PCI 58h [1] = 0. Either pin 2 or pin 54 may be used for SPDIFO.
PCGNT#	54	I	PC/PCI grant input. Enable PC/PCI by setting PCI 50h [10:8] = 010. Select PCGNT# from pin 54 by setting Allegro_Base+58h [6] = 1. Either pin 54 or pin 63 may be used for PCGNT#.
VOLDN#		I	Hardware volume control (volume down). Used in combination with pin 53 (VOLUP#). Hardware volume control is enabled by setting PCI 52 [7] = 1. Pins 53:54 is selected for hardware volume control by setting PCI 52h [5] = 0. Pins 44:45 may also be used for hardware volume control.
VAUX	55	I	3.3 volt V_{AUX} voltage supply input. If V_{AUX} is not supported, then V_{AUX} (pin 55) should be connected to VCC and V_{AUXD} (pin 62) should be pulled down.
SDI2	56	I	External AC-link serial data input. Select secondary Codec by enabling Allegro_Base+38h [5] = 1.
GPIO8		I/O	General purpose input/output
OSCI	57	I	49.152 MHz crystal input
OSCO	58	O	49.152 MHz crystal output
SRESET2#	59	O	Reset output for AC-Link interface. Select secondary Codec by enabling Allegro_Base+38h [5] = 1.
GPIO3		I/O	General purpose input/output
SDFS2		O	Serial data frame sync output for AC-Link interface. Select secondary Codec by enabling Allegro_Base+38h [5] = 1.
GPIO9	60	I/O	General purpose input/output
(note)			If a pull-down resistor is used on this pin, the ES1988 is configured as a multifunction device (audio-modem). Otherwise, the ES1988 is configured as a single function audio-only device.
SCLK2	61	O	Serial clock for AC-link interface. Select secondary Codec by enabling Allegro_Base+38h [5] = 1.
GPIO10		I/O	General purpose input/output
SDO2		O	External AC-link serial data output. Select secondary Codec by enabling Allegro_Base+38h [5] = 1.
GPIO11		I/O	General purpose input/output
VAUXD	62	I	V_{AUX} detect. During the reset period, the V_{AUXD} pin is driven high to indicate ACPI support in the D3$_{cold}$ state, and is driven low to indicate ACPI is not supported in the D3$_{cold}$ state. If V_{AUX} is not supported, then V_{AUX} (pin 55) should be connected to VCC and V_{AUXD} (pin 62) should be pulled down.

Name	Number	I/O	Description
PCGNT#		I	PC/PCI grant input. Enable PC/PCI by setting PCI 50h [10:8] = 010. Select PCGNT# from pin 63 by setting Allegro_Base+58h [6] = 0. Either pin 54 or pin 63 may be used for PCGNT#.
GT0#	63	O	Grant to PCI master. GTO# is enabled by setting PCIx2 arbiter bits PCI 58h [0] = 1 and PCI 58h [11] = 1. Select GT0#/GSO from pin 63 by enabling PCI 58h [10] = 1. Pin 51 may also be used as GT0#/GSO.
GS0		O	Grant select 0 output to control external quick switch to grant PCI master phase. GSO is enabled by setting PCIx2 arbiter bit PCI 58h [0] = 1 and PCI 58h [11] = 0. Select GS0/GT0# from pin 63 by enabling PCI 58h [10] = 1. Pin 51 may also be used as GT0#/GSO.
GPIO12		I/O	General purpose input/output
PC_BEEP	64	I	PC Speaker input
PHONE	65	I	Mono input
CD_L	66	I	CD-audio input: left channel
CD_GND	67	I	CD-audio input: ground
CD_R	68	I	CD-audio input: right channel
MIC	69	I	Microphone input
LINE_IN_L	70	I	Line input: left channel
LINE_IN_R	71	I	Line input: right channel
AVDD[2:1]	83, 72	I	Analog supply voltage, 5V
AVSS[2:1]	82, 73	I	Analog ground
VREF	74	O	Reference voltage
AFILT[2:1]	76:75	O	Anti-aliasing filter cap for the ADC channel
CAP[2:1]	78:77	O	ADC and DAC reference caps
LINE_OUT_L	79	O	Line output: left channel
LINE_OUT_R	80	O	Line output: right channel
MONO_OUT	81	O	Mono output
RXD	84	I	MIDI receive data input. Enable MIDI I/O (MPU-401 I/O) by setting PCI 40h [3] = 1.
GPIO1		I/O	General purpose input/output
TXD		O	MIDI transmit data output. Enable MIDI I/O (MPU-401 I/O) by setting PCI 40h [3] = 1.
GPIO2	85	I/O	General purpose input/output
(note)			If a pull down resistor is used on this pin, then pin 2 is enabled for multifunctionality (IDSEL, RO#, SPDIFO, and PCREQ#). Otherwise, pin 2 may only be used for IDSEL.
RST#	86	I	PCI reset input
INT#	87	O	Interrupt request output
PCICLK	88	I	PCI bus clock input
GNT#	91	I	Bus master grant input
REQ#	92	O	Bus master request output

STRAPPING OPTIONS

Pin number	Strapping	Description
Pin 60 (SDFS2/GPIO9)	low	ES1988 is configured as a multifunction device (audio-modem).
	open or high	ES1988 is configured as a single function device (audio only).
Pin 62 (SDO2/GPIO11/VAUXD)	low	ES1988 does not support V_{AUX} (D3 cold "Wake Up on Ring").
	high	ES1988 supports V_{AUX} (D3 cold "Wake Up on Ring").
Pin 85 (GPIO2/TXD)	low	Pin 2 is in multifunction mode. See Pin Description for Pin 2.
	open or high	Pin 2 is only being used for ID Select.

Typical Configurations

Application	Pin number	Strapping	Description
Audio Only Design	60	open or high	Design is audio only. Single PCI configuration space is available. Function 0 with device ID 1988h.
	62	low	Design does not support "Wake Up on Ring". Pin 55 (VAUX) is connected to VCC.
	85	open or high	Pin 2 is used for ID Select.
		low	Pin 2 is used for multifunction. ID Select is configured through AD24. Pin 2 may be used for PCREQ#, S/PDIF output, or RO#..
Audio - Modem Designs	60	low	Design is an audio-modem combo. Two PCI configurations are available with separate device ID's (audio: function 0 with device ID 1988h, modem: function 1 with device ID 1989h).
	62	high	Design supports "Wake Up on Ring" through V_{AUX}. Pin 55 (VAUX) is connected to V_{AUX}.
		low	Design does not support "Wake Up on Ring". Pin 55 (VAUX) is connected to VCC.
	85	open or high	Pin 2 is used for ID Select.
		low	Pin 2 is used for multifunction. ID Select is configured through AD24. Pin 2 may be used for PCREQ#, S/PDIF output, or RO#..

FUNCTIONAL PIN GROUPING

Function	Pins	Pin Number
AC-Link Interface Pins: Digital Docking	SDI2*	56
	SRESET2*	59
	SDFS2*	60
	SCLK2*	61
	SDO2*	62
AC-Link Interface Pins: MC'97 CODEC	MC97_DI*	53
	SRESET2*	59
	SDFS2*	60
	SCLK2*	61
	SDO2*	62
ACPI / V_{AUX} Pins	PME#*	54
	V_{AUX}	55
	V_{AUXD}*	62
Audio Interface Pins	SPDIFO* (Digital)	2, 54
	I2SDATA* (Digital)	52
	PCBEEP (Analog)	64
	PHONE (Analog)	65
	CD_L (Analog)	66
	GD_GND (Analog)	67
	CD_R (Analog)	68
	MIC (Analog)	69
	LINE_IN_L (Analog)	70
	LINE_IN_R (Analog)	71
	LINE_OUT_L (Analog)	79
	LINE_OUT_R (Analog)	80
	MONO_OUT (Analog)	81
	RxD* (MIDI)	84
	TxD* (MIDI)	85
Bus Master Interface Pins	RO#	2, 52
	GTO#/GSO	51, 63
Clock and Generation Pins	CLKRUN#*	39
	ECLK*	45
	I2SCLK*	50
	OSCI	57
	OSCO	58
	SCLK2*	61
	PCICLK	88

Function	Pins	Pin Number
DAA/Speakerphone Interface Pins	PHONE	65
	MIC	69
	LINE_OUT_L	79
	LINE_OUT_R	80
	MONO_OUT	81
EEPROM Interface Pins	ECS *	39
	EDOUT *	43
	EDIN *	44
	ECLK *	45
Gameport Interface Pins	GD0*	42
	GD1*	43
	GD2*	44
	GD3*	45
	GD4	46
	GD5*	47
	GD6*	48
	GD7*	49
General-Purpose I/O Pins	GPIO1 *	84
	GPIO2 *	85
	GPIO3 *	59
	GPIO4 *	50
	GPIO5 *	51
	GPIO6 *	52
	GPIO7 *	53
	GPIO8 *	56
	GPIO9 *	60
	GPIO10 *	61
	GPIO11 *	62
	GPIO12 *	63
	GPIO13 *	47
	GPIO14 *	48
	GPIO15 *	49
Hardware Volume Interface Pins	VOLUP#*	44, 53
	VOLDN#*	45, 54
I^2S Interface Pins	I2SCLK*	50
	I2SLR*	51
	I2SDATA*	52

Function	Pins	Pin Number
PCI Bus Interface Pins	IDSEL	2
	AD[31:0]	93:100, 4:11, 22:29,31:38
	C/BE[3:0]#	1,13, 20 ,30
	FRAME#	14
	IRDY#	15
	TRDY#	16
	DEVSEL#	17
	STOP#	18
	PAR	19
	CLKRUN#	39
	RST#	85
	INT#	86
	PCICLK	88
	GNT#	91
	REQ#	92
PC/PCI Interface Pins	PCREQ#	2, 53
	SIRQ#	50
	PCGNT#	54, 63
Power and Ground Pins	VCC (3.3V digital supply voltage)	12, 41, 90
	AVDD[2:1] (5.0V analog supply voltage)	72, 83
	V_{AUX}	55
	VREF	74
	GND (digital ground)	3, 21, 40, 89
	AVSS[2:1] (analog ground)	73, 82
S/PDIF Interface Pins	SPDIFO*	2, 54

* These pins share more than one function.

BLOCK DIAGRAMS
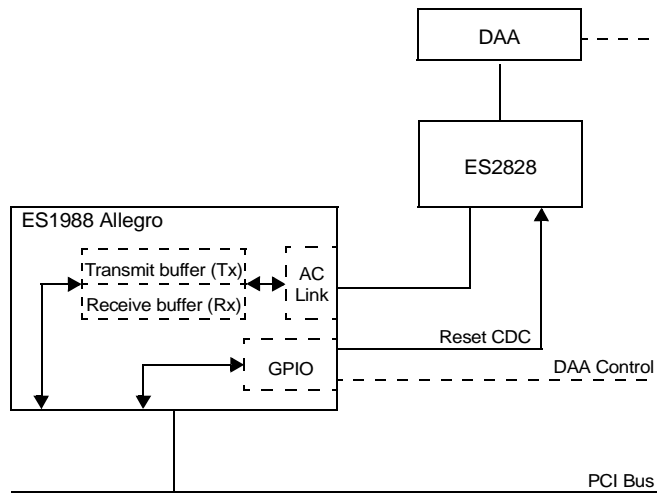
Chip definitions:
ES1988 Allegro: 100-pin PCI audio-modem accelerator
ES2828: single 16-bit modem CODEC

Figure 2 ES1988 System Block Diagram
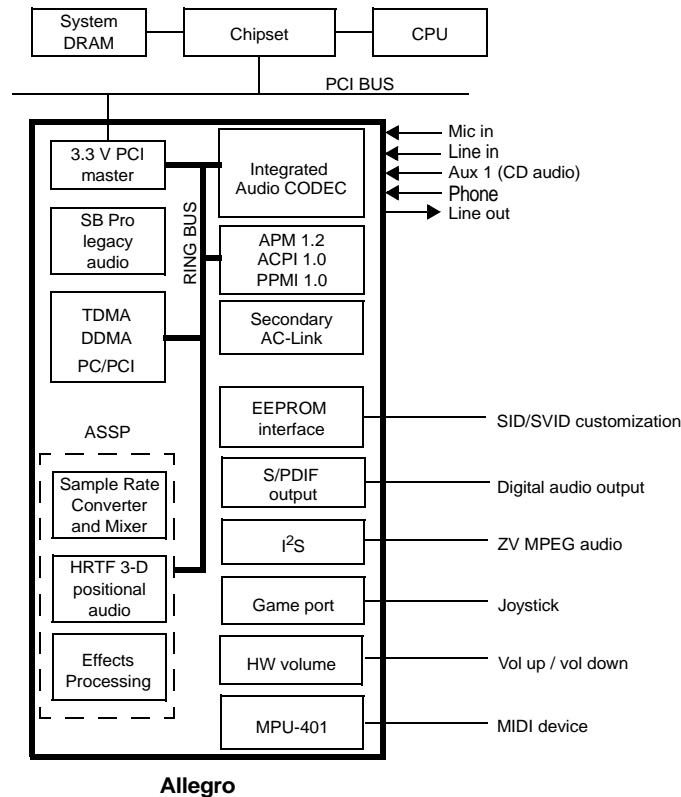
Allegro
Figure 3 ES1988 Device Block Diagram

FUNCTIONAL DESCRIPTION

The ES1988 Allegro PCI audio accelerator is a single-chip audio-modem solution. The ES1988 provides a flexible audio-modem I/O interface to both an audio subsystem and a HSP modem subsystem while serving as a bi-directional buffer for data transmission and reception. The ES1988 also incorporates both an integrated AC'97 Codec and a AC'97 Extension 2.1 compliant link to interface with a secondary, external AC'97 Codec and/or an MC'97 compliant modem AFE. This allows the system integetrator to integrate features of on-system high performance audio and modem, with digital docking capabilities while using only a single PCI load.

The ES1988 includes the following subsystems:

Audio Subsystems

- **AC'97 Compliant Audio Codec** – all analog input and outout interconnect via the embedded Codec.

- **AC'97 Link** – provides interface to an external, secondary Codec and/or an MC'97 compliant Codec.

- **ASSP** -- FM emulation, sample rate conversion, digital mixing, 3D audio and special effects are performed by the embedded asynchronous specific signal processor.

- **Dual game port** – integrated dual game port for two joysticks.

- **EEPROM Interface** – serial port connection from an EEPROM for Subsystem ID and Subsystem Vendor ID.

- **FIFO** – RAM for a 128-word FIFO data buffer as memory-mapped I/O for I/O processing.

- **Hardware volume control** – 2 pushbutton inputs with internal pull-up devices for up/down/mute that can be used to adjust the master volume control.

  The mute input is defined as the state when both up and down inputs are low simultaneously.

- **I^{2}S Zoom Video serial port** – supports sample rates up to 48 kHz for MPEG audio.

- **MPU-401 serial port** – asynchronous serial port for MIDI devices such as a music keyboard input.

- **Oscillator** – circuitry to support an external crystal.

- **PCI bus interface** – provides interface to 3.3 volt PCI bus signals. The PCI 2.2 compliant interface supports bus master/slave.

- **Record source and input volume control** – input source and volume control for recording. The recording source can be selected from one of four choices:

  – Aux 1 (CD-audio)

  – Line In

  – Mic In

  – Phone

Modem Subsystems

- ACPI-compliant power management controller

- Analog and digital sigma-delta modulators

- ADC and DAC signal channels

- Anti-aliasing filters

- Decimation FIR filter

- Interpolation IIR filter

PCI Interface

The ES1988 audio accelerator features a number of dedicated registers for handling of audio data and for handling modem data during an online session and for power management. These registers include dual PCI configuration registers and power management registers.

The setting of bit 7 of the Header Type register at index 0Eh determines how the PCI configuration space of the ES1988 shall be used. Set at 0, the ES1988 is a single-function, audio-only device. Set at 1, however, the ES1988 becomes a multi-function audio-modem device for combo configurations. When configured as a multi-function device, the audio and modem sections will have their own PCI configuration registers.

Table 1 lists the dual sets of registers.

Table 1   Dual Registers in the ES1988 Architecture

Dual Register Name	Register Index
PCI Configuration Register	
ES1988 I/O Space Base Address	10h,11h (R/W)
Interrupt Line	3Ch (R/W)
Power Management	
Next-Item Pointer	C1h (R)
Power Management Capabilities	C2h, C3h (R)
Power Management Control/Status	C4h (R)
PME Control	C5h (R/W)

Memory Architecture

The ES1988 includes 3K x 16 words of on-chip program RAM and 3K x 16 words of on-chip data RAM in its Application Specific Signal Processor (ASSP) module, which serves as the device's program and data memory. Additionally, the ES1988 contains a 128-word RAM as memory-mapped I/O for I/O processing.

Figure 1 details the Allegro memory architecture.
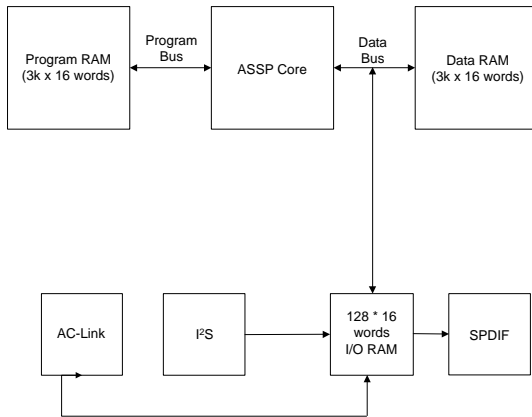
ASSP Memory Mapping

The Allegro uses the following data and program memory maps:

- Program Memory

  0h - BFFh (3K SRAM)

- Data Memory

  500h - 5FFh (I/O SRAM)

  1000h - 1 BFFh (3K SRAM)

  2000h - 2BFFh (3K logical SRAM for FM)

ASSP I/O RAM

In the Allegro, the 128 x 16 I/O RAM is implemented by ping-pong buffer to reduce interrupt latency. The ASSP can read from I/O port 8014h to determine which bank is available. Bit 3 means the 48K Even bank status, while Bit 7 means I^{2}S Even bank status. If the relative bit is 1, the Odd bank is available. If the relative bit is 0, the Even bank is available. The ASSP can read data in from either the I^{2}S or AC-Link at the addresses listed in Table 2.

Table 2   Memory Address (Input)

Even Bank	Odd Bank	Signal Name
0500 ~ 0503	0540 ~ 0543	ADC left
0504 ~ 0507	0544 ~ 0547	ADC right
0508 ~ 050b	0548 ~ 054b	docking ADC left
050c ~ 050f	054c ~ 054f	docking ADC right
0510 ~ 0513	0550 ~ 0553	I^{2}S_L
0514 ~ 0517	0554 ~ 0557	I^{2}S_R

The ASSP can write data out to either the AC-Link or S/PDIF at the addresses listed in Table 3.

Table 3   Memory Address (Output)_

Even Bank	Odd Bank	Signal Name
0520 ~ 0523	0560 ~ 0563	DAC_L (slot 3)
0524 ~ 0527	0564 ~ 0567	DAC_R (slot 4)
0528 ~ 052b	0568 ~ 056b	Center (slot 6)
052c ~ 052f	056c ~ 056f	L SUR (slot 7)
0530 ~ 0533	0570 ~ 0573	R_SUR (slot 8)
0534 ~ 0537	0574 ~ 0577	LFE_SUR (slot 9)
0538 ~ 053b	0578 ~ 057b	S/PDIF L
053c ~ 053f	057c ~ 057f	S/PDIF R

S/PDIF Interface

The ES1988 allows the designer a choice in routing the S/PDIF output to either pin 2 or pin 54 (pin 54 is the default pin). To select SPDIFO at pin 2, GPIO9 pin 85 is pulled down and the SPDIFO bits (Allegro Configuration B, register 53h, Bit [0] = 1 and User Configuration A, register 58h, Bit [1] = 1) are enabled.

The S/PDIF output of the ES1988 transfers audio data in a digital format linked to the data's sampling rate. Each left or right channel of digital data is transferred in a 32-bit subframe, with two subframes making up one frame of data transferred at the 48 kHz sample rate.

Each channel's subframe consists of a single 2's complement digital sample up to 20 bits wide in conjunction with 12 bits of control data. 192 frames of data make up a single data block.

The S/PDIF output works in conjuction with several control/status registers located in the I/O space of the ASSP core. These registers control the functionality of the interface as well as transfer the non-audio data located in the S/PDIF data stream to and from the DSP.

Integrated AC'97 Codec

The integrated AC'97 Codec in the ES1988 integrates a low-pass continuous anti-aliasing filter, a 16-bit resolution analog-to-digital converter (ADC), and a 16-bit digital-to-analog converter. Figure 4 presents a block diagram of its composition.
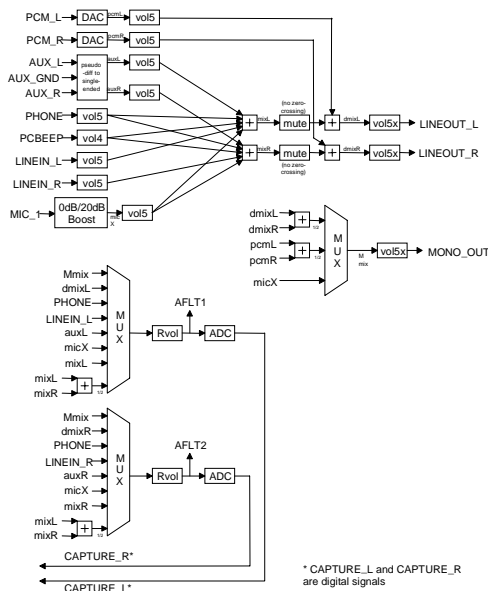
Figure 4   Integrated AC'97 Codec Functional Block Diagram

The major functions of the integrated AC'97 Codec include A/D and D/A conversion of modem/voice signal data and to provide the interface and control logic to transfer data between its serial I/O terminals and Allegro. The integrated AC'97 Codec consists of ADC and DAC signal processing channels and the associated digital controls for each channel. The two channels operate synchronously so that data reception at the ADC channel and data transmission from the DAC channel occur during the same time interval.

AC-Link Interface

The additional AC-Link of the ES1988 is a bi-directional, fixed rate serial PCM digital stream that handles both multiple input and output data streams and control register accesses using a time division multiplexed scheme.

Codec Data Output Framing

The ES1988 AC-Link architecture supports five outgoing data streams, each with 20-bit sample resolution. Specifically, Slots 0, 1, 2, 3, and 4 as defined by the AC'97 Rev. 2.1 spec are supported and comprise the ES1988 SDATA_OUT bi-directional data frame.

Figure 5 shows the output and input frames supported by the integrated AC'97 Codec.
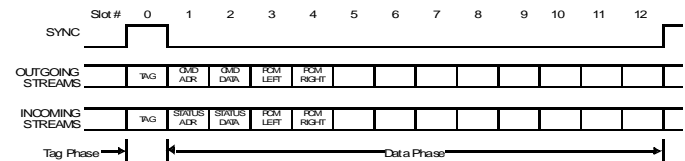
Figure 5   The ES1988 Bi-directional Data Frame

Slot 0: Tag

Within Slot 0, the first bit is a global bit that flags the validity for the entire data frame. If the valid frame bit is a 1, the current data frame contains at least one slot time of valid data. The next five bit positions sampled indicate which of the corresponding five time slots contain valid data.

Slot 1: Command Address Port

The command address port controls features and monitors status of AC'97 functions.   The command address port bit assignments are listed in Table 4.

Table 4   Slot 1 Command Address Bits and Functions

Bit	Function	Description
19	Read/Write command	1 = read; 0 = write
18:12	Control Register Index	64 16-bit locations, addressed on even byte boundaries.
11:0	Reserved	Stuffed with zeroes.

Slot 2: Command Data Port

The command data port delivers 16-bit control register write data in the event the current command port operation is a write cycle. If the current command port operation is a read cycle, the entire time slot must be stuffed with zeros by the digital controller. The command data port bit assignments are listed in Table 5.

Table 5   Slot 2 Command Data Bits and Functions

Bit	Function	Description
19:4	Control Register Write Data	Stuffed with zeroes if current operation is a read.
3:0	Reserved	Stuffed with zeroes.

Slot 3, PCM Playback Left Channel and Slot 4, PCM Playback Right Channel

Audio output frame slot 3 is the composite digital audio left playback stream. Audio output frame slot 4 is the composite digital audio right playback stream. In a typical "games compatible" PC, this slot is composed of standard PCM (*.wav) output samples digitally mixed with music synthesis output samples. If a sample stream of resolutions less than 20 bits is transferred, the Allegro stuffs all trailing non-valid bit positions within this time slot with zeros.

Codec Data Input Framing

The ES1988 AC-Link architecture supports five incoming data streams with 20-bit sample resolution. Specifically, Slots 0, 1, 2, 3 and 4 as defined by the AC'97 Rev. 2.1 spec are supported and comprise the ES1988 SDATA_IN bi-directional data frame.

Slot 0: Tag

Within Slot 0, the first bit is a global bit that flags whether the integrated AC'97 Codec is in the Codec Ready state or not. If the Codec Ready bit is a 0, the integrated AC'97 Codec is not ready for normal operation. This condition is normal following the deassertion of power on reset, for example, while the Allegro's voltage references settle.

When the Codec Ready bit is a 1, the Control and Status Registers and the AC-Link are fully operational. The ES1988 must then further probe the Powerdown Control/ Status register to determine if any further subsections, if any, are ready.

Before putting the integrated AC'97 Codec into operation, the ES1988 polls the first bit in the data input frame to ensure the integrated Codec registers have gone Codec Ready.

Once the integrated Codec registers are Codec Ready, the next five bit positions sampled by the ES1988 indicate which of the corresponding slots are assigned to input data streams, and that they contain valid data.

A new data frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the integrated Codec samples the assertion of SYNC.

This falling edge marks the time when both sides of AC-Link are aware of the start of a new data frame. On the next rising of BIT_CLK, the integrated Codec transitions SDATA_IN into the first bit position of Slot 0 (Codec Ready bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK.

Slot 1: Status Address Port

The status address port controls features and monitors status of AC'97 functions.

The status address port bit assignments are listed in Table 6.

Table 6   Status Address Port Bit Assignments

Bit	Function	Description
19	Reserved	Stuffed with zeroes.
18:12	Control Register Index	Echo of register index for which data is being returned.
11:2	SLOTREQ bits	Refer to Appendix A of the AC'97 Component Spec.
1:0	Reserved	Stuffed with zeroes.

Slot 2: Status Data Port

The command data port delivers 16-bit control register read data in the event the current command port operation is a write cycle. If the current command port operation is a read cycle, the entire time slot must be stuffed with zeros by the digital controller. The status data port bit assignments are listed in Table 7.

Table 7   Status Port Data Bit Assignments

Bit	Function	Description
19:4	Control Register Read Data	Stuffed with zeroes if tagged invalid.
3:0	Reserved	Stuffed with zeroes.

Slot 3, PCM Record Left Channel and Slot 4, PCM Record Right Channel

Audio input frame slot 3 is the left channel output of AC'97's input mux, post-ADC. Audio input frame slot 4 is the right channel output of AC'97's input mux, post-ADC. AC'97 ships out its ADC output MSB first. There are no non-valid bit positions.

Hardware and Master Volume Control

Two external pins, VOLUP# and VOLDN#, can be connected to external momentary switches to ground to implement hardware master volume controls. Pressing one of these buttons produces a low signal to one of the inputs and thereby changes the master volume.

MUTE is emulated by the state where both VOLUP# and VOLDN# inputs are low simultaneously. The up and down buttons produce a single step change in volume when they are first pressed. If these buttons are held down, they enter a fast-scrolling mode. The two inputs have debounce circuitry within the ES1988. Hold each input low or high for it to be recognized as a valid button press. A software option allows the debounce time to be reduced.

The two inputs have debounce circuitry within the ES1988. Setting bits 6 and 7 in the Allegro Configuration B register at index 52h/53h enables hardware volume control and the reduced debounce feature. The ES1988 also includes the option to select from two pairs of VOLUP# and VOLDN# pins via bit 5 of the User Configuration B register at index 52h. Setting bit 5 at 1 enables the VOLUP# and VOLDN# inputs to be routed to pins 53 and 54. Setting bit 5 at 0 enables the inputs to be re-routed to pins 44 and 45.

Peripheral Interfacing

I^{2}S Serial Interface

The I^{2}S input pins I^{2}SDATA, I^{2}SCLK, and I^{2}SLR are used for a serial interface to an external device and are multiplexed with other functions. Refer to Table 8 for a description of the I^{2}S interface pins. Set bit 15 of the Allegro_Base+37h register to 1 to enable the I^{2}S input pins. A typical application of the I^{2}S serial interface is MPEG audio. See Figure 6.
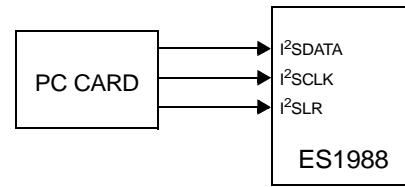
Figure 6 I^{2}S Implementation in ES1988

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Table 8   I^{2}S Interface Pins

Pin	Description
I^{2}SDATA	Serial data for I^{2}S interface. This pin has an internal pull-down to GNDD.
I^{2}SCLK	Serial shift clock for I^{2}S interface. This pin has an internal pull-down to GNDD.
I^{2}SLR	Left/Right signal for I^{2}S interface. This pin has an internal pull-down to GNDD.

I^{2}S Serial Interface Software Enable

Bit 0 of mixer register 7Fh enables the data bus connection to the I^{2}S interface.

I^{2}S Serial Interface Timing

Three signals are used for I^{2}S:

I^{2}SCLK   The shift clock. The maximum rate is 6.4 MHz. The minimum number of I^{2}SCLK periods per I^{2}SLR period is 32. Any number greater than or equal to 32 is acceptable.

I^{2}SLR   Sample synchronization signal. The maximum sample rate is 50 kHz.

I^{2}SDATA   Serial data.

Within the ES1988, I^{2}SLR and I^{2}SDATA are sampled on the rising edge of I^{2}SCLK.

Joystick / MPU-401 Interface

MPU-401 UART Mode

There is one MIDI interface in the ES1988, an MPU-401 "UART mode" compatible serial port.

Joystick / MIDI External Interface

The joystick portion of the ES1988 reference design is identical to that on a standard PC game control adaptor or game port. The PC compatible joystick can be connected to a 15-pin D-sub connector. It supports all standard PC joystick-compatible software. If the system already has a game card or port, remove the game card.

DOS Game Compatibility

ISA DMA

To emulate ISA DMA on the PCI bus, the ES1988 can employ three different protocols:

TDMA	Transparent DMA, a chipset independent mechanism
DDMA	Distributed DMA, must be supported by the PCI chipset
PC/PCI DMA	PC to PCI DMA, must be supported by the PCI chipset

Once one of the three DMA protocols is set up, the ES1988 is seen as an ISA device.

TDMA

In TDMA, the ES1988 snoops PCI bus transactions to a legacy DMA controller device then performs a PCI bus master transaction to complete DMA.

DDMA

In DDMA, the central resource (PCI chipset) includes a DMA remap engine. All transactions to legacy DMACs are remapped to each client (such as the ES1988) by the remap engine. The ES1988 then performs a PCI bus master transaction.

PC/PCI DMA

In PC/PCI DMA, the central resource (PCI chipset) performs PC/PCI cycles, which use sideband signals to the standard PCI bus. The ES1988 then acts as a slave device during DMA.

ISA IRQ

The ISA IRQ is edge triggered while PCI IRQ is level sensitive. By configuring the IRQ policy bits in PCI Configuration register 50h, the ES1988 can emulate ISA IRQ. Setting bit 15 of Legacy Audio Control register (index 40h) to 0 allows the ES1988 to decode legacy audio addresses.

Selecting DMA/IRQ Policy

Because PCI chipsets do not all support the same DMA protocols, DMA policy should be selected according to the chipset in use. To find out which DMA policy to use, contact your ESS FAE. DMA policy is configured in PCI Configuration register 50h, bits [10:8].

HSP Modem Operation

The Allegro is configureable to function as an HSP modem device, precluding the need for an external DSP or modem data pump in the modem subsystem design. In host modem operation, the Allegro has two basic functions related to modem operation:

1. Bidirectional circular buffer:
   - Received data is sampled by the ES2828 modem AFE at various frequencies: 7.2, 8.0, 9.0, 9.6, 10.287, and 16 kHz depending on the sample rate. The sample rate (16 bits per sample) is put into the receive buffer before being sent to the host.
   - Transmitted data from the host (PCI bus) is put into the transmit buffer in synchronization with the receive buffer.
   - Every six samples (configurable), the Allegro checks the buffer and generates an interrupt to the host if the buffer has 12 (configurable) or more samples and lets the host perform I/O read/write. The interrupt is level sensitive.

2. DAA control
   - To make a modem functional, the following control lines are recommended: (US/NA version only; no handset; universal DAA support)

OH	Off hook
RI	Ring indicator
CID	Caller ID (for voice applications)
DAA_PM	DAA power control
Reset_CDC	Reset ES2828 CODEC

   - Full DAA interface

D3$_{cold}$ Wake-Up On Ring

Figure 7 graphically describes the basic D3$_{cold}$ wake-up on ring operation with the ES1988 involved.
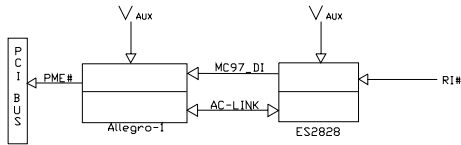
Figure 7   D3$_{cold}$ Wake-Up On Ring Sequence

During D3$_{cold}$, V$_{AUX}$ supplies minimal power to the ES1988 to allow it to power-up the system when voltage from a ring event is detected. When a ring event occurs on RI, MC97_DI goes high and triggers the SDATA_IN signal in the digital controller, which goes high until a warm reset is applied to the MC'97 part (such as the ES2828).

A PME# event is generated by the ES1988, which in turn generates a PCI bus master request for power. When the bus master starts to send more power to the digital controller, it also sends along a PCI RST# signal to reset the system registers on all devices and peripherals. Before the signal completes its system-wide reset, the PME_EN and PME_ST bits in the control register of the digital controller need to have their bit values updated by MC97_DI's rising edge from the ES1988.

The ES1988 must not pass on the Reset signal to the integrated AC'97 Codec when the PME# event has occurred by the initiation of the integrated AC'97 Codec, as a Reset signal will reset all device registers and prevent the digital controller from powering up. The RI, MC97_DI and the PRD:PRA related logic are all powered by V$_{AUX}$.

Ring In Enable

When the ES1988 is paired with an MC'97 part such as the ES2828 modem AFE, setting bit 0 of the Allegro Configuration B register at index 52h/53h enables the RING_IN function to be received at the muxed RXD/GPIO1 pin 84. The muxed TXD/GPIO2 pin 85 is also enabled to complete the I/O path with the ES2828 and with the DAA interface.

Data and Fax Modes

In audio-modem configuration, the ES1988 supports all data modem standards up to 56 Kb/s. Modulations and data rates conform to the following standards:

- ITU V.90
- ITU V.34
- ITU V.32*bis*
- ITU V.32
- ITU V.22*bis*
- ITU V.22
- ITU V.21
- Bell 212A
- Bell 103

V.42/MNP 2-4 error correction and V.42*bis*/MNP 5 data correction reduce error transmission and improve data throughput. The default AT command set is TIES (Time Independent Escape Sequence).

The Hayes escape sequence, which is time dependent, is optionally supported. Both escape sequences are universally accepted by communications software programs.

The Fax AT command set is compatible with EIA/TIA-578 Class 1 and Class 2 standards. Fax transmit and receive speeds up to 14.4 Kb/s are available. Fax modulations and data rates conform to the standards appearing in Table 9 and Table 10.

Table 9   Fax Modes Supported

ITU Mode	Data Rate (kb/s)	Modulation
V.17	14.4 12.0 9.6 7.2	TCM TCM TCM TCM
V.21ch2	0.3	FSK
V.27ter	4.8 2.4	DPSK DPSK
V.29	9.6 7.2 4.8	QAM QAM QAM

Table 10   Data Modes Supported

ITU Mode	Data Rate (kb/s)	Modulation
V.90 V.34	56 33.6 31.2 28.8 26.4 24.0 21.6 19.2 16.8 14.4 12.0 9.6 7.2 4.8 2.4	PCM TCM TCM TCM TCM TCM TCM TCM TCM TCM TCM TCM TCM TCM TCM
V.32*bis*	14.4 12.0 9.6 7.2 4.8	TCM TCM TCM TCM TCM
V.32	9.6 9.6 4.8	TCM QAM QAM
V.22*bis*	2.4	QAM
V.22	1.2	DPSK
V.21	0.3	FSK
Bell 212A	1.2	DPSK
Bell 103	0.3	FSK

Support for Modem Wakeup

Support for PME# event generation, modem wakeup, ring input status, time stamp for ring and DAA data I/O is provided by the ES1988 at the register level.

- Modem Wakeup Control (Allegro_Base+40h/41h): This register handles PME# event generation from ring input whenPME#_RI bit 4 (Allegro_Base+40h) is enabled.

- DAA Data I/O Port (Allegro_Base+50h/+51h): This register handles ring data input from the integrated AC'97 Codec.

- Ring input status bit (Allegro_Base+42h/43h)

- Time stamp 0 and 1 for ring (Allegro_Base+4Ah/4Bh and Allegro_BAse+4Ch/4Dh)

PCI CONFIGURATION REGISTERS

Vendor ID   (00h, 01h, R)

Vendor ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Vendor ID	Identifies ESS as the manufacturer of this device. The ID for ESS is 125Dh.

Device ID   (02h, 03h, R)

Device ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Device ID	Identifies the ES1988 Allegro. The ID 1988h is assigned by ESS Technology, Inc.

Command   (04h, 05h, R/W)

0													BM	0	IO
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:3	–	Read-only. Returns 0 when read.
2	BM	Bus Master enable/disable. 1 = Enable bus master. 0 = Not bus master.
1	–	Read-only. Set to 0.
0	IO	I/O Space access enable/disable. 1 = Enable I/O space access. 0 = Disable I/O space access.

Status   (06h, 07h, R)

Status															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	–	Read-only. Returns 0290h when read.

Revision ID   (08h, R)

Revision ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Revision ID	Identifies the revision of this device. The ID 10h is assigned by ESS Technology, Inc.

Programming Interface Identifier   (09h, R)

Programming interface identifier							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	PII	Identifies the programming interface of this device. The ID 00h indicates a default interface.

Sub-Class Code   (0Ah, R)

Sub-Class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	SCC	Identifies the type of sub-class of this device. The ID 00h indicates a multimedia device (audio-modem). The ID 01h indicates an audio device. The ID 80h indicates a modem device.

Base Class Code   (0Bh, R)

Base class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	BCC	Identifies the type of base class of this device. The ID 04h indicates an audio device. The ID 07h indicates a communication device (modem).

Cache Line Size   (0Ch, R/W)

Cache line size							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CLS	Identifies the cache line size of this device as 00h.

Latency Timer (0Dh, R/W)

Latency timer					0		
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:3	LT	Number of clocks times 8 (read-write for audio. Returns 0 when read for modem).
2:0	–	Read-only. Returns 0s when read.

Header Type (0Eh, R)

SM	Configuration space layout						
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	SM	Single-/multi-function device. The ES1988 supports both audio-only single-function and multi-function audio-modem device operations. 1 = Multi-function device when used in an audio-modem configuration. 0 = Single-function device when used in an audio-only configuration.
6:0	CSL	Configuration space layout. Read-only. Defines layout for bytes 10h and up of the PCI configuration space header. ES1988 supports a 00h header type.

BIST Capability (0Fh, R)

Built-in self test capability							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	BIST	Built-in self test capability is 00h.

Allegro I/O Space Base Address (Audio: Function 0) (10h, 11h, R/W)

IOSB[15:8]								0							ISI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:8	IOSB[15:8]	I/O space base address. 128-word I/O space.
7:1	–	Reserved. Always write 0.
0	ISI	I/O space indicator. Hardwired to 1.

Allegro I/O Space Base Address (Modem: Function 1) (10h, 11h, R/W)

IOSB[15:8]								0							ISI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:8	IOSB[15:8]	I/O space base address. 128-word I/O space.
7:1	–	Reserved. Always write 0.
0	ISI	I/O space indicator. Hardwired to 1.

Subsystem Vendor ID (2Ch, 2Dh, R/W)

Subsystem Vendor ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SVID	Read/write protected. Default = 125Dh. Customizable through register programming by EEPROM or system BIOS. Writable when PCI 50h [0] = 1.

Subsystem ID (2Eh, 2Fh, R/W)

Subsystem ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SID	Read/write protected. Default = 1988h. Customizable through register programming by EEPROM or system BIOS. Writable when PCI 50h [0] = 1..

Capability Pointer (34h, R)

Capability pointer							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CP	This register provides a pointer into the PCI configuration header where the PCI power management register block resides. PCI header doublewords at C0h and C4h contain the power management registers. This register is read-only and returns C0h when read.

Interrupt Line
(Audio: Function 0)   **(3Ch, R/W)**

Interrupt line							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	IL	Interrupt line routing information. Indicates which system interrupt pin the ES1988 is connected to. The POST software writes the routing information to the Interrupt Line register as the system is initialized and configured. The value in this register depends on the system architecture. In x86-based PC systems, the values of 0 to 15 correspond with IRQ numbers 0 through 15, and the values from 16 to 254 are reserved. The value of 255 (Allegro's default power-up value) signifies either "unknown" or "no connection" for the system interrupt. The default value is FFh. Bits [4:0] are read/write. Bits [7:5] = bit [4].

Interrupt Line
(Modem: Function 1)   **(3Ch, R/W)**

Interrupt line							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	IL	Interrupt line routing information. Indicates which system interrupt pin the ES1988 is connected to. The POST software writes the routing information to the Interrupt Line register as the system is initialized and configured. The value in this register depends on the system architecture. In x86-based PC systems, the values of 0 to 15 correspond with IRQ numbers 0 through 15, and the values from 16 to 254 are reserved. The value of 255 (ES1988's default power-up value) signifies either "unknown" or "no connection" for the system interrupt. The default value is FFh. Bits [4:0] are read/write. Bits [7:5] = bit [4].

Interrupt Pin   **(3Dh, R)**

Interrupt pin							
7	6	5	4	3	2	1	0
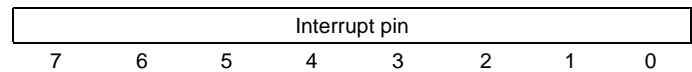
Bit Definitions:

Bits	Name	Description
7:0	IP	Interrupt pin information. Indicates which interrupt pin the ES1988 is using. This register is read-only and returns 01h when read, which indicates INTA#.

Minimum Grant   **(3Eh, R)**

Minimum grant							
7	6	5	4	3	2	1	0
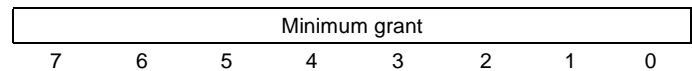
Bit Definitions:

Bits	Name	Description
7:0	MG	Min_Gnt. Identifies the burst period needed. This register is read-only and returns 02h when read, which corresponds to 500 ns, and returns 00h for modem.

Maximum Latency   **(3Fh, R)**

Maximum latency							
7	6	5	4	3	2	1	0
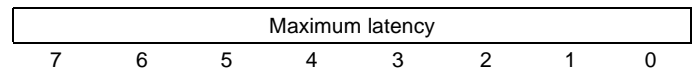
Bit Definitions:

Bits	Name	Description
7:0	ML	Max_Lat. Identifies how often bus access is needed. This register is read-only and returns 18h when read, which corresponds to 6 ms, and returns 00h for modem.

Legacy-Compatible Audio Registers

Legacy Audio Control   (40h, 41h, R/W)

LA	SIR	MIDIIRQ		SBIRQ		DMACH		IA	MQ	MI	GM	FM	SB
15	14	13 12	11	10 9	8	7 6	5		4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	LA	Legacy audio disable. 1 = Disable legacy audio (default). 0 = Enable legacy audio.
14	SIR	Serial IRQs enable. 1 = Enable serial IRQs. 0 = Disable serial IRQs (default).
13:11	MIDIIRQ	MIDI I/O IRQ select. Read-only. Default to 010.

10:8   SBIRQ   Sound Blaster IRQ select.

Bit 10	Bit 9	Bit 8	IRQ Selection
0	0	0	IRQ5 (default)
0	0	1	IRQ7
0	1	0	IRQ9
0	1	1	IRQ10
1	x	x	Reserved

7:6   DMACH   Sound Blaster DMA channel select.

Bit 7	Bit 6	DMA Channel Selection
0	0	Channel 0
0	1	Channel 1 (default)
1	0	Reserved
1	1	Channel 3

Bits	Name	Description
5	IA	I/O address aliasing control. 1 = Enable address aliasing (default). Selects 10-bit I/O. 0 = Disable address aliasing.
4	MQ	MPU-401 IRQ enable. 1 = Enable MPU-401 IRQ (default). 0 = Disable MPU-401 IRQ.
3	MI	MPU-401 I/O enable. 1 = Enable MPU-401 I/O (default). 0 = Disable MPU-401 I/O.
2	GM	Game port enable. 1 = Enable game port (default). 0 = Disable game port.
1	FM	FM synthesis enable. 1 = Enable FM synthesis (default). 0 = Disable FM synthesis.
0	SB	Sound Blaster enable. 1 = Enable Sound Blaster channel (default). 0 = Disable Sound Blaster channel.

Legacy Audio Support

The ES1988 supports the following legacy audio addresses.

Table 11 Supported Legacy Audio Addresses

Legacy Audio Resources	I/O Address Base
Sound Blaster Pro	220h/240h
FM synthesis	388h/289h/38Ah/38Bh
MPU-401	300h/320h/330h/340h
DMA	Channel 0, 1, 3
IRQ	5, 7, 9, 10

Allegro Configuration A   (50h, 51h, R/W)

SBI	PIC1	PIC0	GM	SG	DMAP			PW	IEM	R	M4D	S2	SD	S(V)ID
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	SBI	Sound Blaster IRQ mask. 1 = Set this bit to enable IRQ masking when bit [10] = 1.
14	PCI1	PCI snoop mode 1. 1 = Set this bit in DOS mode when ES1988 PCI IRQ is not assigned to IRQ5/7/9/10.
13	PCI0	PCI snoop mode 0. 1 = Set this bit in DOS mode when ES1988 PCI IRQ is assigned to IRQ5/7/9/10.
12	GM	High-performance game port mode enable. 1 = Enable game port. 0 = Disable game port.
11	SG	Safeguard in TDMA mode, when bits [10:8] = 001. 1 = Set this bit to enable ISA merge during IOR 08h. ISA write-back in AutoDMA mode, when bits [10:8] = 100. 1 = Set this bit to enable ISA write-back in AutoDMA mode.

10:8   DMAP   ISA DMA policy.

Bit 10	Bit 9	Bit 8	DMA Policy
0	0	0	Distributed DMA
0	0	1	Transparent DMA
0	1	0	PC/PCI DMA
0	1	1	Reserved
1	0	0	ISA write-back every 16 transfers
1	0	1	ISA write-back every 4 transfers
1	1	0	ISA write-back every 2 transfers
1	1	1	ISA write-back every transfer

Bits	Name	Description
7	PW	EN_PW. Posted write enable. 1 = Enable ES1988 posted write. 0 = Disable ES1988 posted write.

Bits	Name	Description
6	IEM	Emulate ISA timing on PCI. 1 = Use PCI timing. 0 = Emulate ISA timing.
5	--	Reserved.
4:3	M4D	MPU_401_DECODE.

Bit 4	Bit 3	MPU-401 I/O
0	0	33x
0	1	30x
1	0	32x
1	1	34x

Bits	Name	Description
2	S2	SB240. Sound Blaster decode. 1 = Sound Blaster decode is 24x. 0 = Sound Blaster decode is 22x.
1	SD	Subtractive decoding. Write: 1 = Delay PCI grant by 1 clock during PCI master cycle and enable the detection of PCI subtractive decoding. Read: 1 = Subtractive decoding is detected.
0	SID	Write-enable bit for PCI subsystem ID (SID) and subsystem vendor ID (SVID). 1 = SID and SVID are read/write. 0 = SID and SVID are read-only (default).

Allegro Configuration B   (52h, 53h, R/W)

ICx	CIS	CxS	PMC	CLKSL	SEN	HWV	DHE	HVI	BD	MW	CxS	SPDIF	RIE
15	14	13 12	11	10 9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	ICx	Internal clock multiplier reset enable. 1 = Reset internal clock multiplier. 0 = Release internal clock multiplier.
14	CIS	ES1988 clock input select. 1 = Select the 49.152 MHz clock from the internal clock multiplier. 0 = Select the 49.152 MHz clock from the external crystal oscillator input (OSCI).
13:12	CxS	Clock multiplier mode select.

Bit 2	Bit 13	Bit 12	Mode
0	0	0	Mode 0
0	0	1	Mode 1
0	1	0	Mode 2
0	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5
1	1	0	Mode 6
1	1	1	Mode 7

Bits	Name	Description
11	PMC	Power management control for CLKRUN# enable. 1 = Enable PM control for CLKRUN#. 0 = Disable PM control for CLKRUN#.

Bits	Name	Description
10:9	CLKSL	Clock divider select for Sound Blaster.

Bit 10	Bit 9	Clock Divider
0	0	Divided by 48
0	1	Divided by 49
1	0	Divided by 50
1	1	Reserved

Bits	Name	Description
8	S EN	S/PDIF enable. 1 = Enable S/PDIF output. 0 = Disable S/PDIF output (default).
7	HWV	Hardware volume control enable. 1 = Enable hardware volume control. 0 = Disable hardware volume control.
6	DHE	Reduced debounce for hardware volume control enable. 1 = Enable reduced debounce. 0 = Disable reduced debounce.
5	HVI	Up/down hardware volume button input select. 1 = Select input from pin 44 and 45. 0 = Select input from pin 53 and 54 (default).
4	BD	BIT_CLK Direction of 2nd Codec Interface 1 = Input 0 = Output (default)
3	MW	Writable EEPROM Interface Enable. 1 = Enable writable EEPROM interface. 0 = Disable writable EEPROM interface.
2	CxMS	Clock Multiplier Mode Select. Used along with CxS (bits 13:12) to support eight modes of clock multiplier.
1	SPDIF TM	SPDIF test mode. 1 = Enable SPDIF test mode.
0	RI_E	Ring In Enable. 1 = Enable Ring In from GPIO0 of MC97. 0 = Disable Ring In from GPIO0 of MC97.

ACPI Power Management Registers

ACPI Control A   (54h, 55h, R/W)

12	24	R	SPDIF	GLUE	R	PIF	HV	GPIO	ASSP	SB	FM	XCLK	MIDI	GP	WP
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The ACPI Control A register sets the state (D1 or D2) of the stop clock for each module (12 MHz clocks, 24 MHz clocks, SPDIF, GLUE, PCI interface, hardware volume, modem/GPIO, ASSP interface, FM, clock multiplier, MIDI and game port).

Bit Definitions:

Bits	Name	Description
15	12	ACPI stop clock control for the 12 MHz clock to the serial interface and the secondary Codec output. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
14	24	ACPI stop clock control for the 24 MHz clock to the internal AC97 Codec. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
13	–	Reserved.
12	SPDIF	ACPI stop clock control for SPDIF. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
11	GLUE	ACPI stop clock control for GLUE. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
10	–	Reserved.
9	PIF	ACPI stop clock control for the PCI interface. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
8	HV	ACPI stop clock control for HW volume control. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
7	GPIO	ACPI stop clock control for GPIO. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
6	ASSP	ACPI stop clock control for the ASSP interface. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
5	SB	ACPI stop clock control for Sound Blaster. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
4	FM	ACPI stop clock control for FM. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
3	XCLK	ACPI stop clock control for clock multiplier. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.

Bits	Name	Description
2	MIDI	ACPI stop clock control for MIDI. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
1	GP	ACPI stop clock control for the game port. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
0	–	Reserved.

ACPI Control B   (56h, 57h, R/W)

12	24	R	SPDIF	GLUE	R	PIF	HV	GPIO	ASSP	SB	FM	XCLK	MIDI	GP	WP
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The ACPI Control B register enables the clock at the state (D1 or D2) set for each module in the ACPI Control A register.

Bit Definitions:

Bits	Name	Description
15	12	ACPI stop clock enable for the 12 MHz clock to the serial interface and the secondary Codec output. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
14	24	ACPI stop clock enable for the 24 MHz clock to the internal AC97 Codec. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
13	–	Reserved.
12	SPDIF	ACPI stop clock enable for SPDIF. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
11	GLUE	ACPI stop clock enable for GLUE. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
10	–	Reserved.
9	PIF	ACPI stop clock enable for the PCI interface. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
8	HV	ACPI stop clock enable for hardware volume control. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
7	GPIO	ACPI stop clock enable for GPIO. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
6	ASSP	ACPI stop clock enable for the ASSP interface. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
5	SB	ACPI stop clock enable for Sound Blaster. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.

Bits	Name	Description
4	FM	ACPI stop clock enable for FM. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
3	XCLK	ACPI stop clock enable for clock multiplier. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
2	MIDI	ACPI stop clock enable for MIDI. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
1	GP	ACPI stop clock enable for the game port. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
0	–	Reserved.

User Configuration A (58h, 59h, R/W)

RLE	RE3	EDD	SC	NQS	PMP	MFE	24	3SB	R	CTM	3OB	R	SO	×2
15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0

Bit Definitions:

Bits	Name	Description
15	RE	REQ# Low at D3 State Enable. 1 = Enables driving PCI REQ# low at D3 state.
14	RE3	REQ# Tri-state at D3 State Enable 1 = Enable tri-state of REQ# at D3 state.
13	EDD	EAPD Drive Enable 1 = Enable EAPD signal from internal AC97 Codec. 0 = Disable EAPD signal from internal AC97 Codec .
12	SC	Stop Clock Enable for Crystal Oscillator 1 = Enables stop clock of crystal oscillator at D3 state.
11	QS	Enable external PCI master support without Quick Switch 1 = Enable support.
10	PMP	External PCI Master Pair Select 1 = External PCI Master Pair selected from pin 2 and pin 63. 0 = External PCI Master Pair selected from pin 52 and pin 51 (default).
9	MFE	Multi-Function Enable/Disable 1 = Disable multi-function feature through software. 0 = Enable multi-function feature through software.
8	24	24 MHz clock input. 1 = Select input clock to internal AC97 Codec from divider of external crystal oscillator clock (OSCI/2). 0 = Select input clock to internal AC97 Codec from external crystal oscillator clock (OSCI).

Bits	Name	Description
7	3SB	Tri-state buffer enable. 1 = Tri-state all output buffers. 0 = Don't tri-state buffers.
6	–	Reserved.
5	CTM	AC97 Codec Test Mode Enable 1 = Enable DOS test mode for internal AC97 Codec. 0 = Normal operation. NOTE: SDI signal from internal AC'97 codec will be driven to GD[4] pin 46.
4:2	--	Reserved.
1	SO	1 = Route SPDIF output to IDSEL pin 2. 0 = Route SPDIF output to PME# pin 54 (default). Note: Pin 85 must be pulled down in order to select S/PDIF output to pin 2.
0	PCI ×2	PCI x2 Arbiter Enable. Default = 0. 1 = Enable PCI master support. 0 = Disable PCI master support (default).

User Configuration B (5Ah, 5Bh, R/W)

Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	–	Reserved.

User Configuration C (5Ch, R/W)

Reserved								PMGM	Reserved				PMGS
15	14	13	12	11	10	9	8	7 6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:6	–	Reserved.
5	PMGM	PME# MC97 Enable. 1 = PME# generation enabled from MC97_DI input pin 53.
4:1	–	Reserved.
0	PMGS	PME# SDI2 Enable 1 = PME# generation enabled from SDI2 input pin 56.

Distributed DMA Control 60h, 61h, R/W)

DMA[15:4]												0	0	0	DE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:4	DMA[15:4]	Distributed DMA base address.
3:1	–	Always write 0.
0	DE	Distributed DMA enable. 1 = Enable distributed DMA. 0 = Disable distributed DMA.

Subsystem Vendor ID Shadow (6Ch, 6Dh, R/W)

Subsystem Vendor ID Shadow															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SVID [15:0]	Subsystem Vendor ID Shadow of PCI 2Ch, 2Dh.

Subsystem ID Shadow (6Eh, 6Fh, R/W)

Subsystem ID Shadow															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SID [15:0]	Subsystem ID Shadow of PCI 2Eh, 2Fh.

Capability ID (C0h, R)

Capability ID							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CID	This register identifies the linked list item as the register for PCI power management. This register is read-only and returns 01h when read, which is the unique ID assigned by the PCI SIG for the PCI location of the capabilities pointer and the value.

Power Management Registers

Next-Item Pointer (C1h, R)

Next-Item pointer							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NIP	This register is used to indicate the next item in the linked list of the PCI power management capabilities. Since ES1988 functions only include one capabilities item, this register is read-only and returns 00h when read for audio only.

Power-Management Capabilities (C2h, C3h, R)

PMES					D2S	D1S	Reserved			DSI	R	PMEC	VER		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:11	PMES	PME_Support. This five-bit field indicates the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit [15] = 0. PME# cannot be asserted from $D3_{cold}$. Bit [14] = 1. PME# can be asserted from $D3_{hot}$. Bit [13] = 1. PME# can be asserted from D2. Bit [12] = 1. PME# can be asserted from D1. Bit [11] = 0. PME# cannot be asserted from D0. Value of bits 15:11 Bits 15:11 = 01110. **Audio Only Function 0.** Bits 15:11 =11110. **Modem w/V_{AUX} Function 1.**
10	D2S	D2S. This bit indicates that this function supports the D2 power management state. 1 = D2 power management is supported.
9	D1S	D1S. This bit indicates that this function supports the D1 power management state. 1 = D1 power management is supported.
8:6	–	Reserved. Bits 8:6 = 000 **Audio Only Function 0.** Bits 8:6 = 010 **Modem w/V_{AUX}, Function 1.**
5	DSI	The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. Always 1.
4		Reserved.
3	PMEC	PME clock. This bit indicates that no PCI clock is required for the function to generate PME#. Value of bit 3 = 0.
2:0	VER	Version. This 3-bit field indicates that this function complies with Revision 1.0 of the PCI Power Management Interface specification. Always 010.

Power-Management Control/Status (C4h, R)

0	0	0	0	0	0	PWR STATE	
7	6	5	4	3	2	1	0

The default value of this register 00h. This register determines and changes the current power state of the ES1988 function. The contents of this register are not affected by the internally-generated reset caused by the transition from the $D3_{hot}$ to D0 state.

Bit Definitions:

Bits	Name	Description
7:2	–	Bits [7:2] are read-only and return 0 when read.
1:0	PS	Power state. This 2-bit field is used both to determine the current power state of a function, and to set the function into a new power state.

Bit 1	Bit 0	Power State
0	0	D0
0	1	D1
1	0	D2
1	1	$D3_{hot}$

PME Control (C5h, R/W)

PME ST	0	0	0	0	0	0	PME EN
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	PME ST	PME# status. Read for PME# Status 1 = PME# is active. 0 = PME# is inactive. Write 1 to clear status bit.
6:1	–	Bits [6:1] are read-only and return 0 when read.
0	PME EN	PME# enable. 1 = Enable PME. 0 = Disable PME.

ALLEGRO I/O REGISTERS

Host Interrupt Control   **(Allegro_Base+18h, +19h, R/W)**

AR	Reserved			PGE	R	CE	R	HIE	R	DIE	Reserved		MIE	SIE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	AR	ES1988 software reset enable. 1 = Enable ES1988 software reset. 0 = Disable ES1988 software reset.
14:11	–	Reserved.
10	PGE	Hardware volume control to PME# generation enable.
9	–	Reserved.
8	CE	CLKRUN# generation test mode enable. 1 = Enable CLKRUN# generation all the time. 0 = Disable CLKRUN# generation.
7	–	Reserved.
6	HIE	Hardware volume control interrupt enable. 1 = Enable hardware volume control interrupt. 0 = Disable hardware volume control interrupt.
5	RIE	Ring interrupt enable 1 = Enable ring interrupt. 0 = Disable ring interrupt.
4	DIE	ASSP software interrupt enable. 1 = Enable ASSP software interrupt. 0 = Disable ASSP software interrupt.
3:2	–	Reserved.
1	MIE	MPU-401 interrupt enable. 1 = Enable MPU-401 interrupt. 0 = Disable MPU-401 interrupt.
0	SIE	Sound Blaster interrupt enable. 1 = Enable Sound Blaster interrupt. 0 = Disable Sound Blaster interrupt.

Host Interrupt Status   **(Allegro_Base+1Ah, R/W)**

R	IHWV	RI	ID	Reserved		4M	BS
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	–	Reserved.
6	IHWV	Hardware volume control interrupt. 1 = Hardware volume control interrupt pending. 0 = No hardware volume control interrupt.
5	RI	Ring indicator interrupt. 1 = Ring interrupt pending. 0 = No ring indicator interrupt.
4	ID	ASSP software interrupt. 1 = ASSP interrupt pending. 0 = No ASSP interrupt.
3:2	–	Reserved.
1	4M	MPU-401 receive interrupt. 1 = MPU-401 receive interrupt pending. 0 = No MPU-401 receive interrupt.
0	BS	Sound Blaster interrupt. 1 = Sound Blaster interrupt pending. 0 = No Sound Blaster interrupt.

Hardware Volume Control   **(Allegro_Base+1Bh, R/W)**

Reserved							Split
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:1	–	Reserved.
0	Split	Hardware volume/counter control register split. 1 = Split volume register from counter register. 0 = Do not split volume from counter register.

Shadow of Mixer Register for Voice   **(Allegro_Base+1Ch, R/W)**

Shadow of Mixer for Voice							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	SMV	Shadow of the mixer register for voice.

HW Volume Control
Counter for Voice　　　(Allegro_Base+1Dh, R/W)

Hardware volume control counter for voice							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	HCV	Hardware volume control counter for voice.

Shadow of Mixer
Register for Master　　　(Allegro_Base+1Eh, R/W)

Shadow of Mixer for Master							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	SMM	Shadow of mixer register for master.

HW Volume Control
Counter for Master　　　(Allegro_Base+1Fh, R/W)

Hardware volume control counter for master							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	HCM	Hardware volume control counter for master.

Game Port Control Registers

Joystick 1 X-Delay　　(Allegro_Base+20h,+21h, R/W)

2A	2B	1A	1B	Delay											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 1 Y-Delay　　　(Allegro_Base+24h,+25h, R/W)

2A	2B	1A	1B	Delay											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 2 X-Delay　　(Allegro_Base+28h,+29h, R/W)

2A	2B	1A	1B	Delay											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 2 Y-Delay　　(Allegro_Base+2Ch,+2Dh, R/W)

2A	2B	1A	1B	Delay											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Codec Control Registers

CODEC Command / Status   (Allegro_Base+30h, W)

RW	AD						
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	RW	Read/Write. 1 = Read cycle. 0 = Write cycle.
6:0	AD[6:0]	CODEC register address.

CODEC Command / Status   (Allegro_Base+30h, R)

0	0	0	0	0	0	0	ST
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:1	–	Reserved. Always read 0.
0	ST	Read/write status. 1 = CODEC register read/write is in progress. 0 = CODEC register read/write is done.

CODEC Data   (Allegro_Base+32h,+33h, W)

WT CODEC Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	WT	16 bits of data to be written to the CODEC.

CODEC Data   (Allegro_Base+34h,+35h, R)

RD CODEC Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	RD	16 bits of data read from the CODEC.

Serial Bus Control Registers

Serial Bus Control A   (Allegro_Base+36h,+37h, R/W)

I²S	R	EIO	ES	LAC SDFS	LAC PME	RAC SDFS	RAC PME	Reserved							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	I²S	I²S input enable. 1 = Enable I²S input. 0 = Disable I²S input.
14	–	Reserved.
13	EIO SRAM	EN_IOSRAM. I/O SRAM enable. 1 = Enable I/O SRAM. 0 = Disable I/O SRAM.
12	ES	Serial AC-link enable. 1 = Enable serial AC-link. 0 = Disable serial AC-link.
11	LAC SDFS	Driving SDFS of local AC-link enable. 1 = Enable driving SDFS of local AC-link. 0 = Disable driving SDFS of local AC-link.
10	LAC PME	Driving PME from SDI of local AC-link. 1 = Enable driving PME from SDI of local AC-link. 0 = Disable driving PME from SDI of local AC-link.
9	RAC SDFS	Driving SDFS of remote AC-link enable. 1 = Enable driving SDFS of remote AC-link. 0 = Disable driving SDFS of remote AC-link.
8	RAC PME	Driving PME from SDI of remote AC-link. 1 = Enable driving PME from SDI of remote AC-link. 0 = Disable driving PME from SDI of remote AC-link.
7:0	–	Reserved.

Serial Bus Control B (Allegro_Base+38h, R/W)

MC_INT	SSPE	CDC2	SPDIF	ITB	R	CDC ID	
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	MC_INT	MC Interrupt enable. 1 = Enable MC interrupt to ASSP. 0 = Disable MC interrupt to ASSP.
6	SBMIF	1 = Enable Sound Blaster module interface. 0 = Disable Sound Blaster module interface.
5	CDC2	1 = Enable second AC-link. 0 = Enable single AC-link.
4	SPDIF	1 = Enable S/PDIF function. 0 = Disable S/PDIF function.
3	MSS	Modem Slot Select Enable 1 = Select MC97_DI for modem slot. 0 = Select SDI1 for modem slot.
2	–	Reserved.

1:0 CDC ID Second CODEC ID.

Bit 1	Bit 0	CODEC ID
0	0	Reserved.
0	1	AC-Link.
1	0	MC 97.
1	1	Reserved.

SDO Output Destination Control (Allegro_Base+3Ah, R/W)

I/O	HS	L2DAC	PCM R/LF	PCM CLS	L1DAC	PCM L/R	CA
15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0

Bit Definitions:

Bits	Name	Description

15:14 I/O I/O control output.

Bit 15	Bit 14	Destination
0	0	Local
0	1	Remote
1	0	Mute
1	1	Both

13:12 HS Handset output.

Bit 13	Bit 12	Destination
0	0	Local
0	1	Remote
1	0	Mute
1	1	Both

11:10 L2DAC Line 2 DAC output.

Bit 11	Bit 10	Destination
0	0	Local
0	1	Remote
1	0	Mute
1	1	Both

Bits	Name	Description

9:8 PCM R/LF PCM R_SURR/LFE output.

Bit 9	Bit 8	Destination
0	0	Local
0	1	Remote
1	0	Mute
1	1	Both

7:6 PCM CLS PCM Center/L_SURR output.

Bit 7	Bit 6	Destination
0	0	Local
0	1	Remote
1	0	Mute
1	1	Both

5:4 L1DAC Line 1 DAC output.

Bit 5	Bit 4	Destination
0	0	Local
0	1	Remote
1	0	Mute
1	1	Both

3:2 PCM L/R PCM L/R output.

Bit 3	Bit 2	Destination
0	0	Local
0	1	Remote
1	0	Mute
1	1	Both

1:0 CA Command address output.

Bit 1	Bit 0	Destination
0	0	Local
0	1	Remote
1	0	MC Codec
1	1	Reserved

SDI Input Destination Control (Allegro_Base+3Ch, R/W)

I/O	HS	L2ADC	R	MIC ADC	L1ADC	PCM L/R	SA
15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0

Bit Definitions:

Bits	Name	Description

15:14 I/O I/O status input.

Bit 15	Bit 14	Destination
x	0	Local
x	1	Remote

13:12 HS Handset input.

Bit 13	Bit 12	Destination
0	0	Local
0	1	Remote
1	x	Mute both

11:10 L2ADC Line 2 DAC input.

Bit 11	Bit 10	Destination
0	0	Local
0	1	Remote
1	x	Mute both

Bits	Name	Description
9:8	–	Reserved.

7:6 MIC ADC — MIC ADC input.

Bit 7	Bit 6	Destination
x	0	Local
x	1	Remote

5:4 L1ADC — Line 1 ADC input.

Bit 5	Bit 4	Destination
0	0	Local
0	1	Remote
1	x	Mute both

3:2 PCM L/R — PCM L/R input.

Bit 3	Bit 2	Destination
0	0	Local
0	1	Remote
1	0	Reserved
1	1	Both

1:0 SA — Status address/data input.

Bit 1	Bit 0	Destination
0	0	Local
0	1	Remote
1	0	MC Codec
1	1	Reserved

Modem Wakeup Control   (Allegro_Base+40h,+41h, R/W)

Reserved											PMG_RI	Reserved			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:5	–	Reserved.
4	PMG_RI	1 = Enable PME# generation from ring input.
3:0	--	Reserved

Modem Ring Input Status   (Allegro_Base+42h,+43h, R/W)

Reserved													RIS	R	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:3	–	Reserved.
2	RIS	Ring Input Status Read for ring input status. 1 = Indicates ring input is pulsing. 0 = Ring input is idle. Write 1 to clear the status bit.
1:0	–	Reserved.

Time Stamp 0 for Ring   (Allegro_Base+4Ah,+4Bh, R)

TS0_RI															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	TS0_RI	Time stamp 0 for Ring.

Time Stamp 1 for Ring   (Allegro_Base+4Ch,+4Dh, R)

TS1_RI															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	TS1_RI	Time stamp 1 for Ring.

DAA Data Input / Output Port   (Allegro_Base+50h,+51h, R/W)

DAA Data I/O															RI#
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:1	DDI/O	DAA data input/output to MC'97.
0.	RI#	Ring data input from MC'97.

GPIO Registers

GPIO Data   (Allegro_Base+60h, +61h, R/W)

GPIO data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	GPD	GPIO data.

GPIO Mask   (Allegro_Base+64h, +65h, R/W)

GPIO write mask															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	GPWM	GPIO write mask. 1 = Mask write. 0 = Unmask write.

GPIO Direction   (Allegro_Base+68h, +69h, R/W)

GPIO direction
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	GPD	GPIO direction. 1 = Output. 0 = Input (default).

ASSP Memory Control Registers

ASSP Memory / Index Port   (Allegro_Base+80h,+81h, R/W)

ASSP memory/index
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	AM/I	Host-to-ASSP 16-bit memory index port. Points to 64K word of ASSP memory.

ASSP Memory Port   (Allegro_Base+82h,+83h, R/W)

Reserved		MSS
15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0

Bit Definitions:

Bits	Name	Description
15:2	–	Reserved.
1:0	MSS	DMA memory space selection.

Bit 1	Bit 0	Memory Space
0	x	Reserved
1	0	ASSP program memory
1	1	ASSP data memory

ASSP Data Port   (Allegro_Base+84h,+85h, R/W)

ASSP data
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Each time this register is accessed for a read or write, the ASSP Memory/Index port (Allegro_Base+80h, +81h) is incremented by 1. The index port is 4K word paged and consecutive access cannot cross this 4K word boundary.

Bit Definitions:

Bits	Name	Description
15:0	AD	16-bit data (word) port.

Game Port Address Registers

Game Port Address A   (Allegro_Base+90h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 200h.

Game Port Address B   (Allegro_Base+91h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 201h.

Game Port Address C   (Allegro_Base+92h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 202h.

Game Port Address D   (Allegro_Base+93h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 203h.

Game Port Address E   (Allegro_Base+94h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 204h.

Game Port Address F   **(Allegro_Base+95h, R/W)**

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 205h.

Game Port Address G   **(Allegro_Base+96h, R/W)**

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 206h.

Game Port Address H   **(Allegro_Base+97h, R/W)**

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 207h.

MPU-401 Address Registers

MPU-401 Port Address A   **(Allegro_Base+98h, R/W)**

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 330h.

MPU-401 Port Address B   **(Allegro_Base+99h, R/W)**

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 331h.

MPU-401 Port Address C   **(Allegro_Base+9Ah, R/W)**

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 332h.

MPU-401 Port Address D   **(Allegro_Base+9Bh, R/W)**

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 333h.

Clock Multiplier
Data Port A   **(Allegro_Base+9Ch, +9Dh, R)**

R	7xS			4xS			3xS		
15	14 13 12 11 10	9 8	7 6 5	4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15	–	Reserved.
14:10	7xS	x7 counter status.
9:5	4xS	x4 counter status.
4:0	3xS	x3 counter status.

ASSP Clock Control Registers

ASSP Control A   (Allegro_Base+A2h, R/W)

Reserved	36CLK	Reserved		33/49CLK	Reserved		0WS
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	–	Reserved.
6	36CLK	36 MHz DSP clock select. 1 = Select 36 MHz DSP clock.
5:4	–	Reserved.
3	33/49 CLK	33 MHz or 49.152 MHz ASSP clock select. 1 = Enable 49.152 MHz ASSP clock. 0 = Enable 33 MHz ASSP clock.
2:1	–	Reserved.
0	0WS	ASSP 0-wait state enable. 1 = Enable ASSP 0-wait state. 0 = Disable ASSP 0-wait state.

ASSP Control B   (Allegro_Base+A4h, R/W)

Reserved			CRE	Reserved			ARST
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	–	Reserved.
4	CRE	Clock run/enable. 1 = Stop ASSP clock. 0 = Enable ASSP clock.
3:1	–	Reserved.
0	ARST	ASSP reset/run. 1 = Run ASSP. 0 = Reset ASSP.

ASSP to Host IRQ Status   (Allegro_Base+ACh, R/W)

ASSP IRQ status							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	AIS	ASSP to host software interrupt request status. Read for pending interrupt status. 1 = Interrupt pending. 0 = No interrupt pending. Write 1 to clear pending interrupt request. The bits in this register are set to 1 by ASSP to request interrupts from the host.

INTEGRATED AC'97 CODEC REGISTERS

Basic

Reset   (00h, R)

R	SE4:SE0				Reserved										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Writing any value to this register performs a register reset, which causes all registers to revert to their default values except for the Powerdown Control/Status register.

Bit Definitions:

Bits	Name	Description
15:14	–	Reserved. Always write 0.
13:9	SE4:SE0	Stereo Enhancement enable bits. 1 = All stereo enhancement features enabled.
8:0	–	Reserved. Always write 0.

Master Volume Control   (02h, R/W)

Mute	x		Master volume left				x			Master volume right					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the master playback volume. The maximum setting (00h) corresponds to 0 dB gain, with each step adding -1.5 dB gain. On reset, the default value is 8000h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set Master volume at -∞ dB. 0 = Mute disabled.
14:13	–	Don't care.
12:8	MVL	Sets the volume level for the LINE_OUT_L output.
7:5	–	Don't care.
4:0	MVR	Sets the volume level for the LINE_OUT_R output.

Table 12 Master Volume Control Bits

Mute	MVx4	MVx3	MVx2	MVx1	MVx0	Gain
0	0	0	0	0	0	0 dB
0	0	0	0	0	1	-1.5 dB
0	0	0	0	1	0	-3.0 dB
continued....						
0	1	1	1	1	1	-46.0 dB
1	X	X	X	X	X	- ∞dB

Master Volume Mono   (06h, R/W)

Mute					x							Master volume mono			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the master playback volume for the mono out. The maximum setting (00h) corresponds to 0 dB gain, with each step adding -1.5 dB gain. On reset, the default value is 8000h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set Master volume at -∞ dB. 0 = Mute disabled.
14:5	–	Don't care.
4:0	MN[4:0]	Sets the volume level for mono output.

PC Beep   **(0Ah, R)**

Mute	Reserved										PV3:PV0			X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the level for the PC Beep input. The maximum setting (00h) corresponds to 0 dB gain. Each step up corresponds to approximately 3 dB of gain. The MSB of this register is the mute bit. When this bit is set to 1, the level for that channel is set at - ∞dB.

PC Beep supports motherboard implementations. The intention of routing PC Beep through the mixer is to eliminate the requirement for an on-board speaker. Automatically connecting PC Beep to the LINE_OUT outputs as soon as the part powers up and completes calibration supports the implementation.

The PC Beep - LINE_OUT connection is broken when SYNC is sampled high. The ES1988 will need to route PC Beep to the LINE_OUT outputs via AC-Link control if so desired. On reset, the default value is 8000h.

Table 13 PC Beep Volume Gain

Mute	PV3	PV2	PV1	PV0	Gain
0	0	0	0	0	0 dB
0	0	0	0	1	+3.0 dB
0	0	0	1	0	+6.0 dB
0	0	0	1	1	+9.0 dB
continued....					
0	1	1	1	0	+42.0 dB
0	1	1	1	1	+45.0 dB
1	X	X	X	X	- ∞dB

Analog Mixer Input Gain Registers

These registers control the volume for each of the analog inputs. The maximum setting (00h) corresponds to 12 dB gain. Each step adds -1.5 dB gain down to the minimum -34.5 dB attenuation (1Fh).

Table 14 shows the relationship between the volume bits and the gain value for registers 0Ch, 0Eh, 10h and 12h

Table 14 Analog Mixer Input Volume Gain

Mute	GX4	GX3	GX2	GX1	GX0	Gain
0	0	0	0	0	0	12.0 dB
0	0	0	0	0	1	10.5 dB
0	0	0	0	1	0	9.0 dB
continued...						
0	0	1	0	0	0	0 dB
0	0	1	0	0	1	-1.5 dB
0	0	1	0	1	0	-3.0 dB
continued....						
0	1	1	1	1	0	-33.0 dB
0	1	1	1	1	1	-34.5 dB
1	X	X	X	X	X	- ∞dB

Phone Volume   **(0Ch, R/W)**

Mute	x	x	x	x	x	x	x	x	x	x	Phone volume			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the gain and attenuation for the analog phone input. The phone input is a mono input. On reset, the default value is 8008h, which corresponds to 0 dB gain with mute off or on.

Bits Definitions:

Bits	Name	Description
15	Mute	In Extended mode, Mute applies only to the left channel. 1 = Mute enabled. Set Phone volume at -∞ dB. 0 = Mute disabled.
14:5	–	Don't care.
4:0	GN	Analog phone gain support bits 4:0. Sets the volume level for the Phone input.

Mute	GX4	GX3	GX2	GX1	GX0	Gain
0	0	0	0	0	0	12.0 dB
0	0	0	0	0	1	10.5 dB
0	0	0	0	1	0	9.0 dB
continued...						
0	0	1	0	0	0	0 dB
0	0	1	0	0	1	-1.5 dB
0	0	1	0	1	0	-3.0 dB
continued....						
0	1	1	1	1	0	-33.0 dB
0	1	1	1	1	1	-34.5 dB
1	X	X	X	X	X	- ∞dB

MIC Volume (0Eh, R/W)

Mute	x	x	x	x	x	x	x	x	20 dB	x	MIC volume			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the volume for the microphone input. The mic input is a mono input. On reset, the default value is 8008h.

Bits Definitions:

Bits	Name	Description
15	Mute	Mute Bit Enable. 1 = Mute enabled. Set Mic volume at -∞ dB. 0 = Mute disabled.
14:7	–	Don't care.
6	20 dB	1 = 20 dB boost enabled. 0 = 20 dB boost disabled.
5	–	Don't care.
4:0	GN	Sets the volume level for the Mic input.

Mute	GX4	GX3	GX2	GX1	GX0	Gain
0	0	0	0	0	0	12.0 dB
0	0	0	0	0	1	10.5 dB
0	0	0	0	1	0	9.0 dB
continued...						
0	0	1	0	0	0	0 dB
0	0	1	0	0	1	-1.5 dB
0	0	1	0	1	0	-3.0 dB
continued....						
0	1	1	1	1	0	-33.0 dB
0	1	1	1	1	1	-34.5 dB
1	X	X	X	X	X	- ∞dB

Line In Volume (10h, R/W)

Mute	x	x	Line in volume left			x	x	x	Line in volume right		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the Line In volume. On reset, the default value is 8808h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set Line in volume at -∞ dB. 0 = Mute disabled.
14:13	–	Don't care.
12:8	LIL	Sets the volume level for the LINE_IN_L input.
7:5	–	Don't care.
4:0	LIR	Sets the volume level for the LINE_IN_R input.

Mute	GX4	GX3	GX2	GX1	GX0	Gain
0	0	0	0	0	0	12.0 dB
0	0	0	0	0	1	10.5 dB
0	0	0	0	1	0	9.0 dB
continued...						
0	0	1	0	0	0	0 dB
0	0	1	0	0	1	-1.5 dB
0	0	1	0	1	0	-3.0 dB
continued....						
0	1	1	1	1	0	-33.0 dB
0	1	1	1	1	1	-34.5 dB
1	X	X	X	X	X	- ∞dB

CD Volume (12h, R/W)

Mute	x	x	CD volume left			x	x	x	CD volume right		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the CD volume. On reset, the default value is 8808h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set CD volume at -∞ dB. 0 = Mute disabled.
14:13	–	Don't care.
12:8	CDL	Sets the volume level for the CDL input.
7:5	–	Don't care.
4:0	CDR	Sets the volume level for the CDR input.

Mute	GX4	GX3	GX2	GX1	GX0	Gain
0	0	0	0	0	0	12.0 dB
0	0	0	0	0	1	10.5 dB
0	0	0	0	1	0	9.0 dB
continued...						
0	0	1	0	0	0	0 dB
0	0	1	0	0	1	-1.5 dB
0	0	1	0	1	0	-3.0 dB
continued....						
0	1	1	1	1	0	-33.0 dB
0	1	1	1	1	1	-34.5 dB
1	X	X	X	X	X	- ∞dB

PCM Playback Volume Control (18h, R/W)

Mute	x	x	PLL volume left				x	x	x	PLR volume right				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the PCM Out volume. On reset, the default value is 8808h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set PCM Out volume at -∞ dB. 0 = Mute disabled.
14:13	–	Don't care.
12:8	PLL	Sets the volume level for the left channel PCM playback.
7:5	–	Don't care.
4:0	PLR	Sets the volume level for the right channel PCM playback.

Record Select (1Ah, R/W)

x	Record select left			x	Record select right		
15 14 13 12 11	10	9	8	7 6 5 4 3	2	1	0

This register selects record sources for the left and right channel. On reset, the default value is 000h.

Bits Definitions:

Bits	Name	Description
15:11	–	Don't care.
10:8	SL[2:0]	Selects left channel record source:

bit 10 bit 9 bit 8 source
  0   0   0   MIC (default)
  0   0   1   CD in (L)
  0   1   0   mono_mix (output of mono mux before MONO_OUT volume)
  0   1   1   dmix (L) (signal just before LINE_OUT_L volume)
  1   0   0   Line left
  1   0   1   Stereo mix left (without PCM data mixed)
  1   1   0   Mono mix (without PCM data mixed)
  1   1   1   Phone

| 7:5 | – | Don't care. |
| 4:0 | SL[2:0] | Selects right channel record source: |

bit 2 bit 1 bit 0 source
  0   0   0   MIC (default)
  0   0   1   CD in (R)
  0   1   0   mono_mix (output of mono mux before MONO_OUT volume)
  0   1   1   dmix (L) (signal just before LINE_OUT_R volume)
  1   0   0   LINE_IN_R
  1   0   1   Stereo mix left (without PCM data mixed)
  1   1   0   Mono mix (without PCM data mixed)
  1   1   1   Phone

Record Gain   **(1Ch, R/W)**

Mute	x	x	x	Record gain left			x	x	x	x	Record gain right			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register sets the volume level for the record input. The minimum setting (00h) corresponds to 0 dB gain. Each step adds 1.5 dB gain up to the maximum 22.5 dB gain (0Fh). Table 16 shows the relationship between the record volume bits and the gain value for register 1Ch.

On reset, the default value is 8000h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set Record gain at -∞ dB. 0 = Mute disabled.
14:12	–	Don't care.
11:8	GL	Sets the volume level for the Record input.
7:4	–	Don't care.
3:0	GR	Sets the volume level for the Record input.

Mute	GX3	GX2	GX1	GX0	Gain
0	0	0	0	0	0 dB
0	0	0	0	1	1.5 dB
0	0	0	1	0	3.0 dB
continued....					
0	1	1	1	0	21.0 dB
0	1	1	1	1	22.5 dB
1	X	X	X	X	- ∞dB

General Purpose   **(20h, R/W)**

x	x	x	x	x	x	MIX	X	LPBK	x	x	x	x	x	x	x
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls a number of miscellaneous functions. This register should be read before writing to generate a mask for only the bit(s) that need to be changed. On reset, the default value is 0000h.

Bits Definitions:

Bits	Name	Description
15:10	–	Don't care.
9	MIX	Mono Output Select 1 = MIC 0 = Mixer Mono Mux Control

DMS MIX MUX Output

DMS	MIX	MUX Output
0	0	dmix mono mix
0	1	micX
1	x	pcm mono mix

Bits	Name	Description
8	–	Don't care.
7	LPBK	This bit enables loopback of the ADC output to the DAC input without involving the AC-Link. This allows for full system performance measurements. 1 = Enable ADC/DAC loopback mode. 0 = Disable ADC/DAC loopback mode.
6:0	–	Don't care.

Powerdown Control/Status   (26h, R/W)

EAPD	x	PR5:PR0				x	x	x	x	REF	ANL	DAC	ADC
15	14	13	12	11	10 9 8	7	6	5	4	3	2	1	0

This register is used to program powerdown states and monitor subsystem readiness. When the AC-Link "CODEC ready" bit (SDATA_IN slot 0 bit 15) is a 1, it indicates that the AC-Link and the ES1988 control and status registers are fully operational. The ES1988 must check bits 3:0 to determine exactly which subsections are ready. Bits 7:0 are read-only. Writes will have no effect on these bits. Bits 3:0 are all 0 after a cold reset.

As each subsection becomes ready to resume normal operation, the corresponding bit becomes a 1. This register is not affected by a write to the reset register. The integrated AC97 Codec has six powerdown bits that control powerdown operation throughout all of ES1988. The stored value of the EAPD bit (bit 15) is routed to the controller portion of ES1988 to provide powerdown capabilities for the external amplifier section of the standalone AC'97 Codec part.

Bits Definitions:

Bits	Name	Description
15	EAPD	External Amplifier Power Down bit. 1 = Set EAPD high to signal an external amplifier to shut down. 0 = Set EAPD low to signal an external amplifier to turn on (default).
14	–	Reserved
13	PR5	Power down digital section and clock. 1 = Digital section powered down with clock disabled. 0 = Digital section powered up with clock enabled.
12	PR4	1 = Digital section powered down with oscillator enabled. The analog mixer can still function. The 24.576 MHz oscillator still runs. This bit can be cleared by either a cold or a warm reset. The digital section powers up quickly as the oscillator is still running. 0 = Digital section powered up.
11	PR3	1 = Analog mixer powered down (Vref off). In this case, the ADCs, DACs, Mixer, and Vref are also powered down; however, the state of PR2:0 are preserved. 0 = Analog mixer powered up.
10	PR2	This section is powered down when PR3 = 1, but the state of PR2 is preserved. 1 = Analog mixer powered down with reference generator still enabled. 0 = Analog mixer powered up.

Bits	Name	Description
9	PR1	This section is powered down when PR3 = 1, but the state of PR1 is preserved. 1 = PCM out DACs powered down. 0 = PCM out DACs powered up.
8	PR0	This section is powered down when PR3 = 1, but the state of PR0 is preserved. 1 = PCM in ADCs, input volume control, and input mux powered down. 0 = PCM in ADCs and input mux powered up.
7:4	–	READ-ONLY. Don't care.
3	REF	READ-ONLY. VREF is up to nominal level.
2	ANL	READ-ONLY. Analog mixers, etc. ready.
1	DAC	READ-ONLY. DAC section ready to accept data.
0	ADC	READ-ONLY. ADC section ready to transmit data.

Integrated AC'97 Registers - Extended Audio AFE

Extended Audio ID   (28h, R)

R		X			AMAP		X						DRA	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0

This register is used to identify the extended audio features that are supported in addition to the original AC'97 features identified by the Reset register. On reset, the default value is 0002h.

Bits Definitions:

Bits	Name	Description
15:14	–	Reserved.
13:10	–	Don't care.
9	AMAP	AC-Link Slot to Audio DAC Map Select. 1 = AC97 Rev. 2.1 mapping supported. 0 = AC'97 mapping not supported.
8:2	–	Don't care.
1	DRA	Double Rate Audio Select. 1 = Double rate audio supported. 0 = Double rate audio not supported.
0	–	Don't care.

Extended Audio Status and Control　　　(2Ah, R/W)

X														DRA Enable	x
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register is used to test the integrated AC97 Codec. On reset, the default value is 0000h.

Bits Definitions:

Bits	Name	Description
15:2	–	Don't care.
1	DRA Enable	Double Rate Audio Enable. 1 = Double rate audio mode enabled. 0 = Double rate audio mode disabled.
0	–	Don't care.

Vendor Registers

Vendor ID 1　　　　　　　　　　　　　(7Ch, R)

First vendor ID character								Second vendor ID character							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register encodes the first two ASCII character of the vendor ID.

Bits Definitions:

Bits	Name	Description
15:8	F	Encodes the first ASCII character of the vendor ID; 45h = E.
7:0	S	Encodes the second ASCII character of the vendor ID; 83h = S.

Vendor ID 2　　　　　　　　　　　　　(7Eh, R)

Third vendor ID character								x	x	x	x	x	x	x	x
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register encodes the third ASCII character of the vendor ID and the vendor revision number.

Bits Definitions:

Bits	Name	Description
15:8	T	Encodes the third ASCII character of the vendor ID; 83h = S.
7:0	RN	Revision number. Returns 08h when read.

ASSP DMA Registers

Host Memory End Address (Low Word)　　　(ASSPIO_4000h, R/W)

Host Memory End Address (Low Word)															R
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register corresponds to the PCI address [15:1].

Bits Definitions:

Bits	Name	Description
15:1	HMEA (L)	Host Memory End Address (Low Word).
0	–	Reserved. Always write 0s.

Host Memory End Address (High Word)　　　(ASSPIO_4001h, R/W)

Reserved				Host Memory End Address (High Word)											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register corresponds to the PCI address [27:16].

Bits Definitions:

Bits	Name	Description
15:12	–	Reserved. Always write 0s and read back as 0s.
11:0	HMEA (H)	Host Memory End Address (High Word).

ASSP Data Memory End Address (ASSPIO_4002h, W)

ASSP Data Memory End Address															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
15:0	ADMA	ASSP Data Memory End Address.

Host Memory Starting Address/
Current Pointer (Low Word)   (ASSPIO_4003h, R/W)

Host Memory Address/Pointer (Low Word)															R
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

When this register is written to by the ASSP, it means host memory starting address. This register corresponds to PCI address [15:1].

Bits Definitions:

Bits	Name	Description
15:1	HMSA (L)	Host Memory Starting Address (Low Word).
0	–	Reserved. Always write 0s.

When this register is read from by the ASSP, it means current host address pointer. The pointer is updated after each data transfer.

Bits Definitions:

Bits	Name	Description
15:1	–	Current host address pointer.
0	–	Reserved. Always read back as 0s.

Host Memory Starting Address/
Current Pointer (High Word)   (ASSPIO_4004h, R/W)

Reserved				Host Memory Starting Address (High Word)											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

When this register is written to by the ASSP, it means host memory starting address. This register corresponds to PCI address [27:16].

Bits Definitions:

Bits	Name	Description
15:12	–	Reserved. Always write 0s.
11:0	HMSA (H)	Host Memory Starting Address (High Word).

When this register is read from by the ASSP, it means current host address pointer. The pointer is updated after each data transfer.

Bits Definitions:

Bits	Name	Description
15:12	–	Reserved. Always write 0s.
11:0	CHAP	Current host address pointer (corresponding to PCI address [27:16].

ASSP Data Memory Starting
Address/Current Pointer   (ASSPIO_4005h, R/W)

ASSP Data Memory Address/Pointer															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

When this register is written to by the ASSP, it means ASSP data memory starting address.

Bits Definitions:

Bits	Name	Description
15:0	DDMS	ASSP Data Memory Starting Address.

When this register is read from by the ASSP, it means ASSP data memory address pointer. The pointer is updated after each data transfer.

Bits Definitions:

Bits	Name	Description
15:0	–	ASSP data memory address pointer.

DMA Control (ASSPIO_4006h, R/W)

Reserved	AMEAS	HMEAS	DSPINT	R/W	DMACTRL							
15 14 13 12	11	10	9	8	7	6	5	4	3	2	1	0

When this register is written to by the ASSP, host and data memory reads and writes are being monitored. Hardware interrupts are generated as necessary if the address counter crosses the host memory 64K boundary. Bits 10 and 11 are read-only and return host and ASSP data memory end address status when read. Four mechanisms will cause the ASSP DMA hardware interrupt to be generated.

1. Completion of data transfer.
2. The host memory end address has been reached (I/O 4206, bit 11 = 1).
3. The ASSP memory end address has been reached (I/O 4206, bit 10 = 1).
4. The host memory 64K boundary has been crossed (I/O 4206, bit 9 = 1).

Bits Definitions:

Bits	Name	Description
15:10	–	Reserved. Always write 0s.
9	DSPINT	ASSP Crossing 64K Boundary Interrupt Enable. 1 = Enable. 0 = Disable.
8	R/W	ASSP Host Memory Read/Write Enable. 1 = Read ASSP data memory and write host memory. 0 = Read host memory and write ASSP data memory.

Bits	Name	Description
7:0	DMA CTRL	Word transfer counts for one-time DMA kick-off from 1 to 256 words (00h - FFh).

When this register is read from by the ASSP, it means ASSP data memory address pointer. The pointer is updated after each data transfer.

Bits Definitions:

Bits	Name	Description
15:12	–	Reserved. Always write 0s.
11	AMEAS	ASSP Memory End Address Status (read-only). 1 = ASSP memory end address reached. 0 = ASSP memory end address not reached.
10	HMEAS	Host Memory End Address Status (read-only). 1 = Host memory end address reached. 0 = Host memory end address not reached.
9	DSPINT	ASSP Hardware Interrupt Enable. 1 = ASSP hardware interrupt enabled.
8	R/W	ASSP Host Memory Read/Write Enable. 1 = DMA transfer in progress. 0 = DMA transfer complete.
7:0	DMA CTRL	Hold transfer bits as written.

ELECTRICAL CHARACTERISTICS

Table 15 Absolute Maximum Ratings

Ratings	Symbol	Value	Units
Analog supply voltage	V_A	-0.3 to 6.0	V
Digital supply voltage	V_D	-0.3 to 6.0	V
Input voltage	V_{IN}	VD +0.5	V
Operating temperature range	T_A	0 to 70	°C
Storage temperature range	T_{STG}	-40 to 125	°C

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. There are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

ES1988 Recommended DC operating conditions

Table 16 Power Management Characteristics

State	Description	Analog	digital	Unit
D0	Fully operational	70	85	mA
D1	Chip in D1 state with internal Codec DAC and ADC powered down	35	15	mA
D2	Chip in D2 state with internal Codec DAC, ADC, and mixer powered down	10	15	mA
D3$_{hot}$	Chip in D3 state with internal Codec powered down. PCICLK and 49.152 MHz crystal powered on.	0.1	0.2	mA
D3$_{cold}$	Chip in D3 state with internal Codec powered down. PCICLK and 49.152 MHz crystal powered down.	0	0.2	mA

Table 17 DC Operating Condition

Parameter	Definition	Min	Typ	Max	Unit
VDD 3.3V	Digital supply voltage	3.15	3.3	3.45	V
AVD	Analog supply voltage	4.75	5.0	5.25	V
T_{AMB}	Ambient temperature	0	25	70	°C

Table 18 Digital Characteristics

Parameter	Definition	Min	Typ	Max	Unit
	Operating Conditions (V_{DDD} = 3.3 V, T_A = 25 °C)				
V_{IH}	High-level input voltage (TTL-static)	2.0			V
V_{OH}	High-level output voltage (TTL-static)	2.4			V
V_{IL}	Low-level input voltage (TTL-static)	0.4		0.8	V
V_{OL}	Low-level output voltage (TTL-static)			0.4	V
I_{IL}	Low-level input current (V_{IN} = VSS)	-10		10	mA
I_{IH}	High-level input current (V_{IN} = VDD)	-10		10	mA
I_{OZ}	Tristate output leakage current (V_{OUT} = VDD/VSS)	-10		10	mA
C_{IN}	Input capacitance			5	pF
C_{OUT}	Output capacitance			5	pF
I_{OB}	Output current drive (SDATA_IN, BIT_CLK)	-		12	mA

Table 19 ES1988 Analog Characteristics

Parameter	Min.	Typ.	Max.	Units
Full Scale Input Voltage:				
Line Inputs		1.0		
Mic Inputs **a**	-	0.1		
Full Scale Output Voltage:				
Line Output		1.0	-	Vrms
Analog S/N:				
CD to LINE_OUT	85			dB
Other to LINE_OUT	85			dB
Analog Frequency Response **b**	20	-	20K	Hz
Digital S/N **c**				
DAC	80	87		dB
ADC	80	87		dB
Total Harmonic Distortion:				
Line Output **d**	-	0.01	0.02	%
DAC/ADC Frequency Response: **e**				
DAC	0		20K	Hz
ADC	20		20K	Hz
Stop Band:				
DAC	28			kHz
ADC		28		kHz
Transition Band:				
DAC	20			kHz
ADC	20		28	kHz
Stop Band Rejection **f**	-74			dB
Out-of-Band Rejection **g**	-	-74	-	dB
Group Delay (DAC Only = 0.5 ms; ADC Only = 0.21 ms)	-	0.85	-	mS
Power Supply Rejection Ratio (1 kHz)	-	-40	-	dB
Crosstalk Between Input Channels	-	-	-60	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Analog Input Impedance	10	22	-	kΩ
CD Input Impedance		11	-	kΩ
Input Capacitance	-	15	-	pF

CONDITIONS:

T_A = 25°C, AVdd = DVdd = 5.0 V ± 5%; Input Voltage Levels: Logic Low = 0.8 V, Logic High = 2.4 V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10 kΩ / 50 pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB attenuation; tone and 3D disabled)

NOTE:

a) With +20 dB boost on (1.0 V_{rms} with 20 dB boost off).

b) ±1 dB limits

c) The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A wtd" over a 20 Hz to a 20 kHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-Noise ratio).

d) 0 dB gain, 20 kHz BW, 48 kHz sample frequency.

e) ±0.25 dB limits max, ±0.1 dB typical.

f) Stop Band Rejection determines filter requirements to 70 kHz. Out-of-Band Rejection determines audible noise.

g) The integrated Out-of-Band noise generated by the DAC process during normal PCM audio playback over a 28.8 kHz to 100 kHz bandwidth, with respect to a 1 Vrms DAC output
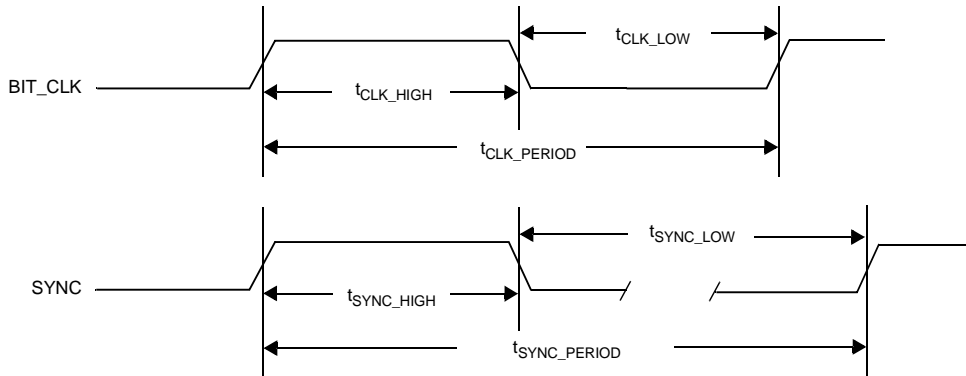
ES1988 TIMING DIAGRAMS
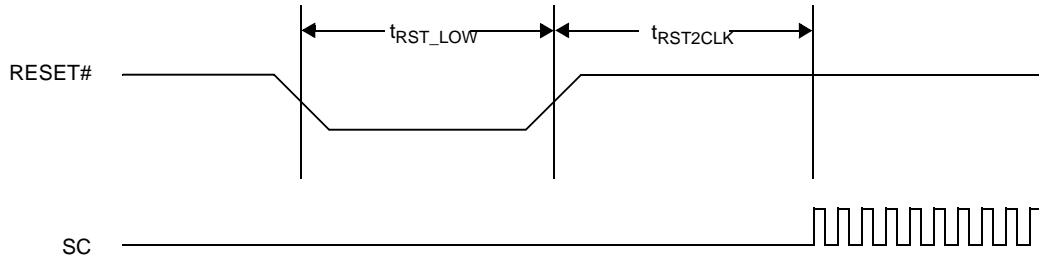
Symbol	Parameter	Min	Typ	Max	Units
t_{RST_LOW}	RESET# active-low pulse width				
	ES2828 Modem AFE	1.0			μs
$t_{RST2CLK}$	RESET# inactive to BIT_CLK start-up delay				
	ES2828 Modem AFE	162.8			ns

Figure 8 Cold Reset
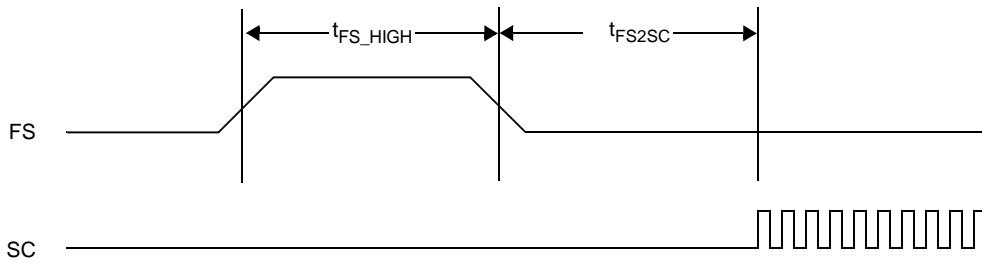
Symbol	Parameter	Min	Typ	Max	Units
t_{FS_HIGH}	SYNC active-high pulse width	1.0			μs
t_{FS2SC}	SYNC inactive to BIT_CLK start-up delay	162.8			ns

Figure 9 Warm Reset

Symbol	Parameter	Min	Typ	Max	Units
	BIT_CLK frequency		12.288		MHz
t_{CLK_PERIOD}	BIT_CLK period		81.4		ns
	BIT_CLK output jitter			750	ps
t_{CLK_HIGH}	BIT_CLK high pulse width*	36	40.7	45	ns
t_{CLK_LOW}	BIT_CLK low pulse width*	36	40.7	45	ns
	SYNC frequency		48.0		kHz
t_{SYNC_PERIOD}	SYNC period		20.8		µs
t_{SYNC_HIGH}	SYNC high pulse width		1.3		ns
t_{SYNC_LOW}	SYNC low pulse width		19.5		ns

* = Worst case duty cycle restricted to 45/55

Figure 10 Clocks
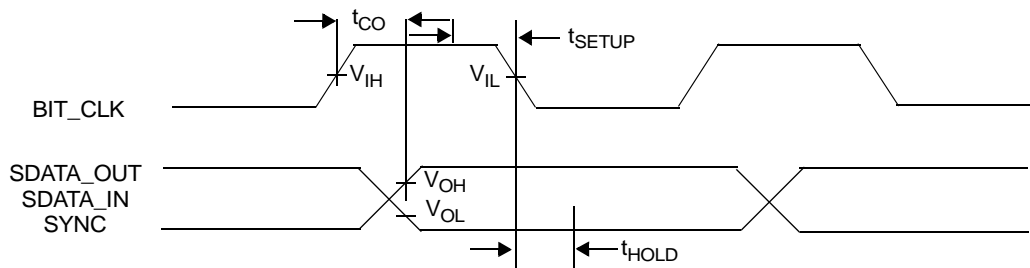
Symbol	Parameter	Min	Typ	Max	Units
	AC-Link Output Valid Delay Timing Parameters				
t_{CO}	Output Valid Delay from rising edge of BIT_CLK			15	ns
	Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output.* Note 2: 50 pF external load.				
	AC-Link Input Setup and Hold Timing Parameters				
t_{SETUP}	Input Setup to falling edge of BIT_CLK	10			ns
t_{HOLD}	Input Hold to falling edge of BIT_CLK	10			ns
	AC-Link Combined Rise or Fall Plus Flight Timing Parameters				
	BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller or Secondary)			7	ns
	SDATA combined rise or fall plus flight time (Output to Input)			7	ns
	Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes.				

Figure 11 Data Output and Input Timing Diagram
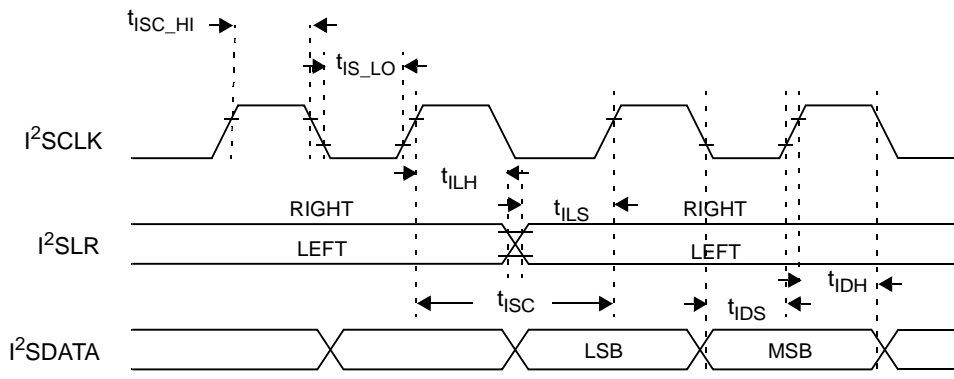
Symbol	Parameter	Min	Typ	Max	Units
t_{ISC}	I^{2}SCLK cycle time	54			ns
t_{IS_HI}	I^{2}SCLK HIGH time	15			ns
t_{IS_LO}	I^{2}SCLK LOW time	15			ns
t_{IDS}	I^{2}DATA setup time	12			ns
t_{IDH}	I^{2}DATA hold time	2			ns
t_{ILS}	I^{2}SLR setup time	12			ns
t_{ILH}	I^{2}SLR hold time	2			ns

Figure 12 I^{2}S Port Timing
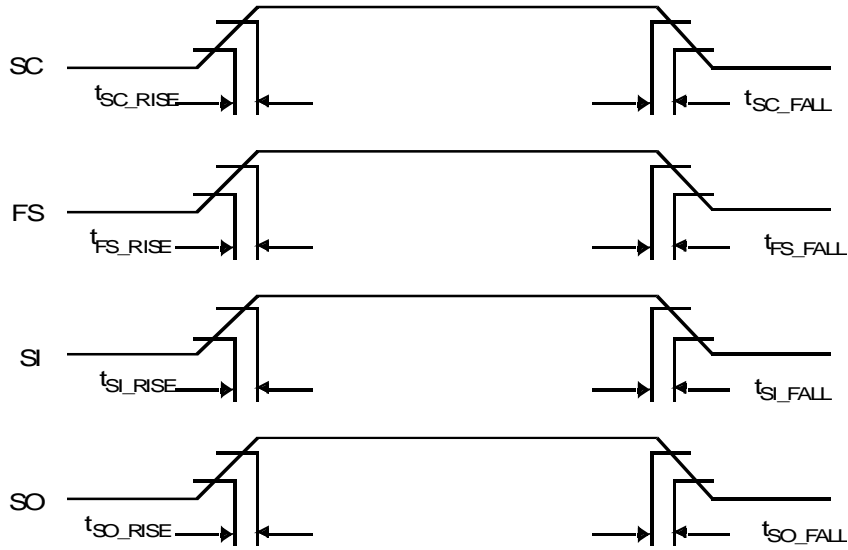
Symbol	Parameter	Min	Typ	Max	Units
t_{SC_RISE}	SC rise time	2		6	ns
t_{SC_FALL}	SC fall time	2		6	ns
t_{FS_RISE}	FS rise time	2		6	ns
t_{FS_FALL}	FS fall time	2		6	ns
t_{SI_RISE}	SI rise time	2		6	ns
t_{SI_FALL}	SI fall time	2		6	ns
t_{SO_RISE}	SO rise time	2		6	ns
t_{SO_FALL}	SO fall time	2		6	ns

Figure 13 Signal Rise and Fall Times
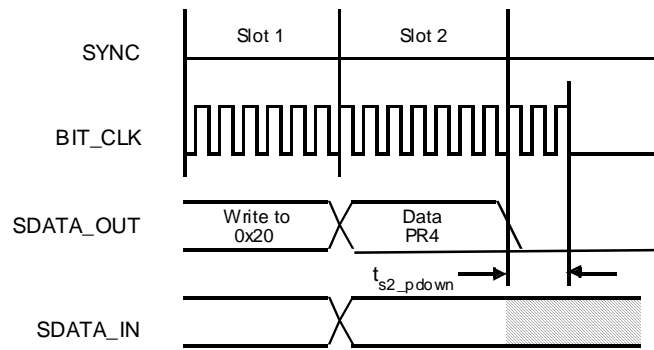
Note: BIT_CLK not to scale.

Symbol	Parameter	Min	Typ	Max	Units
t_{S2_PDOWN}	End of Slot 2 to BIT_CLK, SDATA_IN low			1.0	µs

Figure 14 AC-Link Low Power Mode Timing

MECHANICAL DIMENSIONS
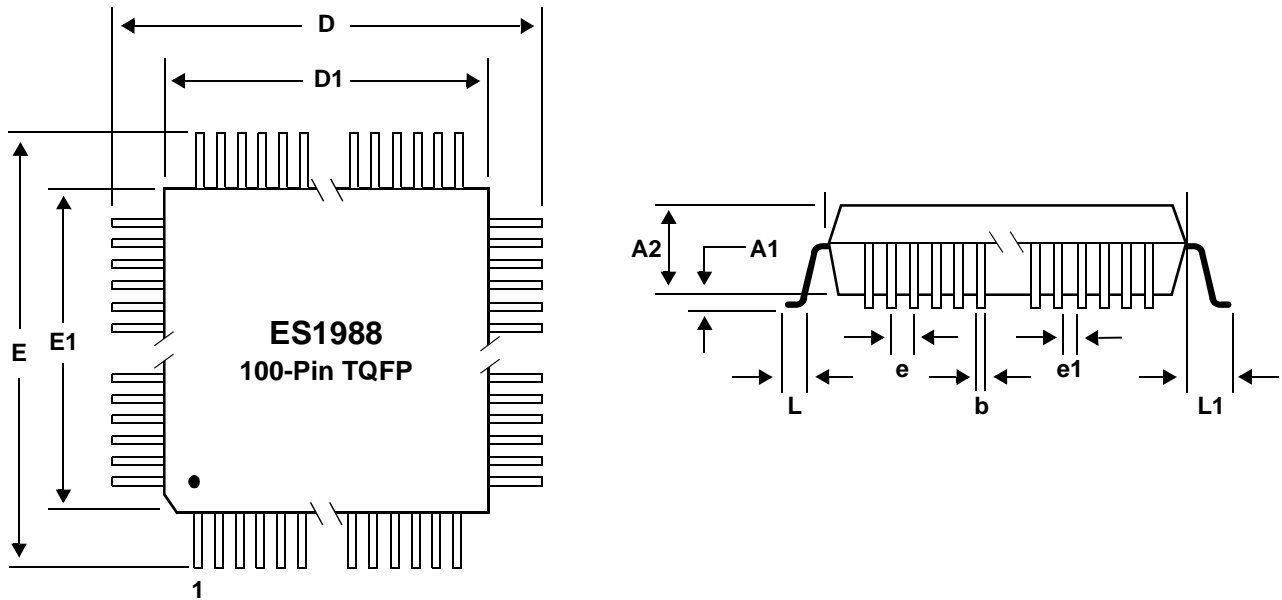
Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	15.75	16.00	16.25
D1	Package's outside, X-axis	13.90	14.00	14.10
E	Lead to lead, Y-axis	15.75	16.00	16.25
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.05	0.10	0.15
A2	Package thickness	1.35	1.40	1.45
b	Lead width	0.17	0.22	0.27
e	Lead pitch	-	0.50	-
e1	Lead gap	0.24	-	-
L	Foot length	0.45	0.60	0.75
L1	Lead length	0.93	1.00	1.07
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	25	-
-	Leads in Y-axis	-	25	-
-	Total leads	-	100	-
-	Package type	-	TQFP	-

Figure 15 Mechanical Dimensions

APPENDIX A: SCHEMATIC EXAMPLES
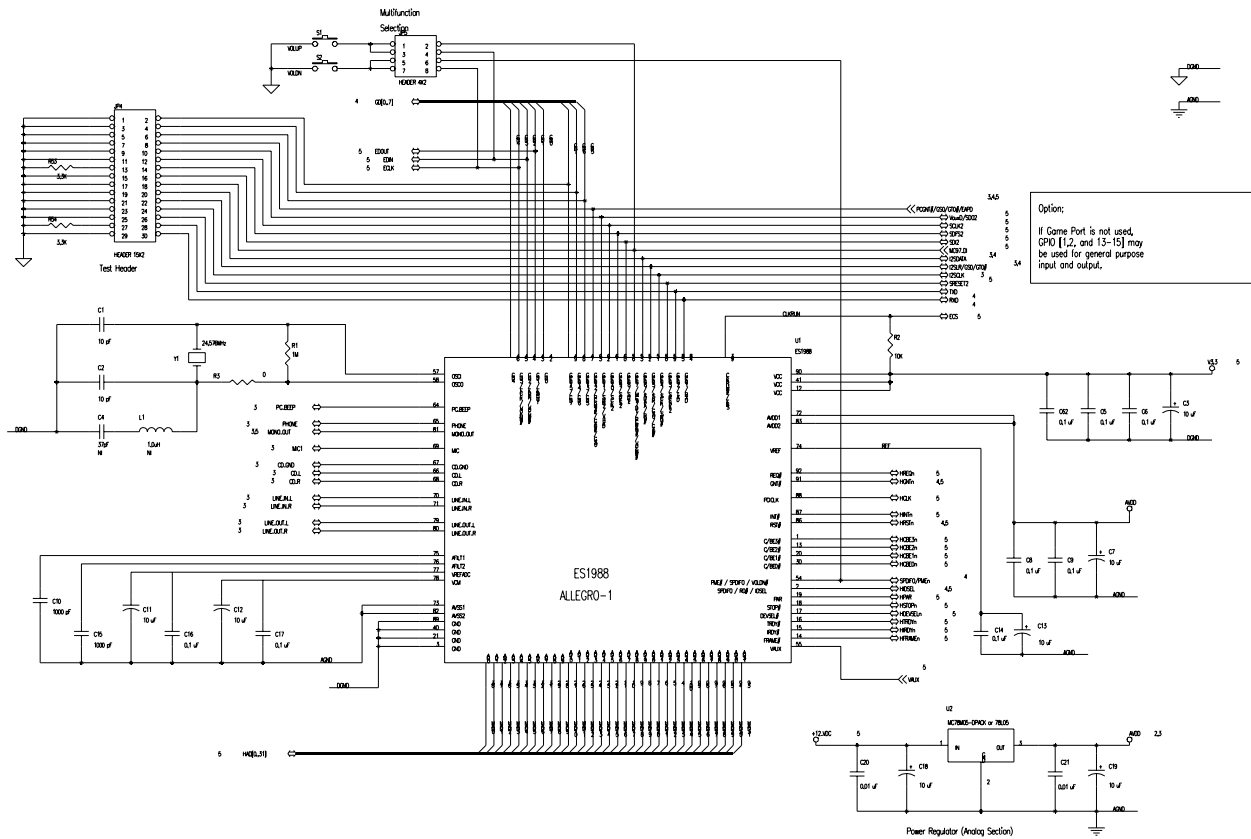
Figure 16 ES1988 Device Interface
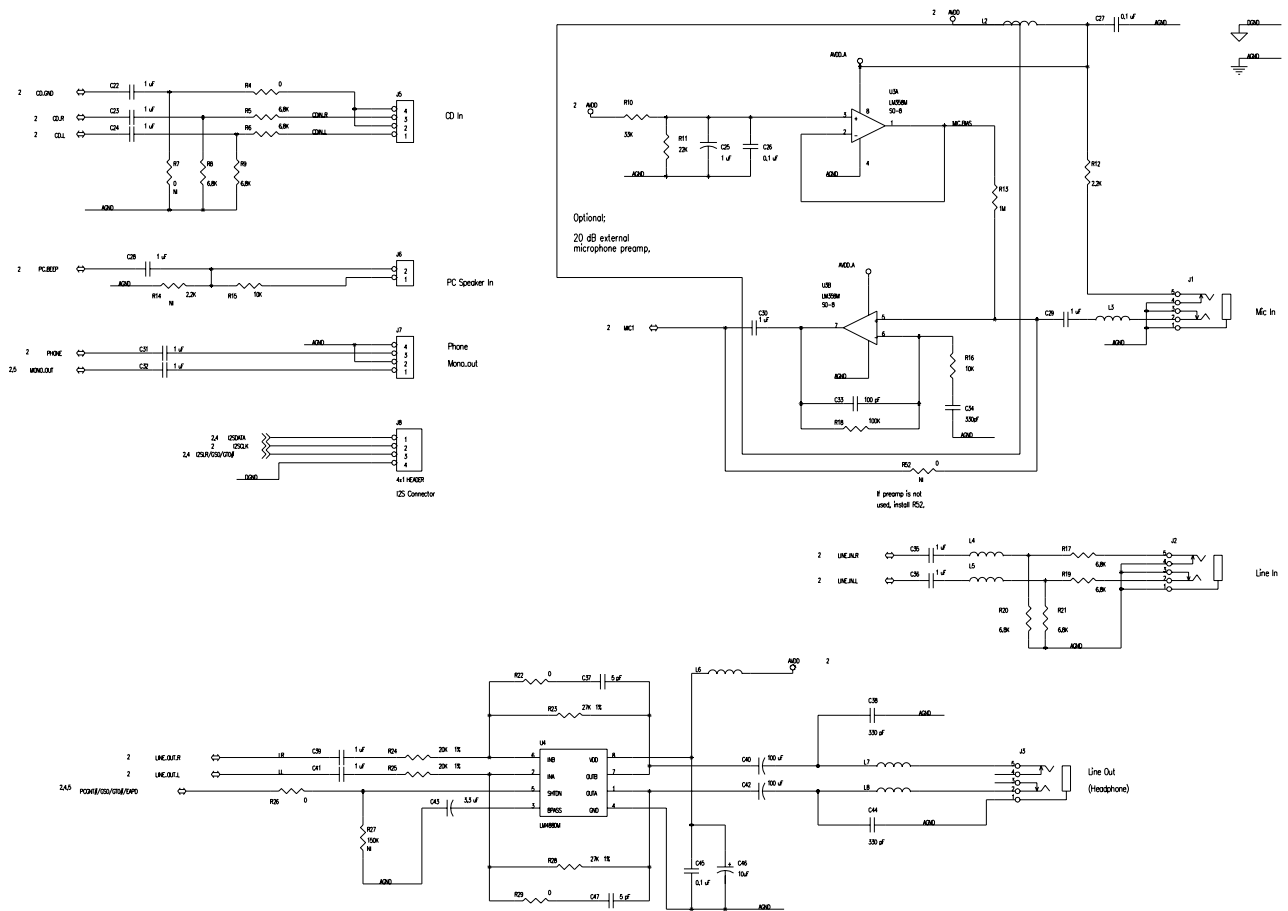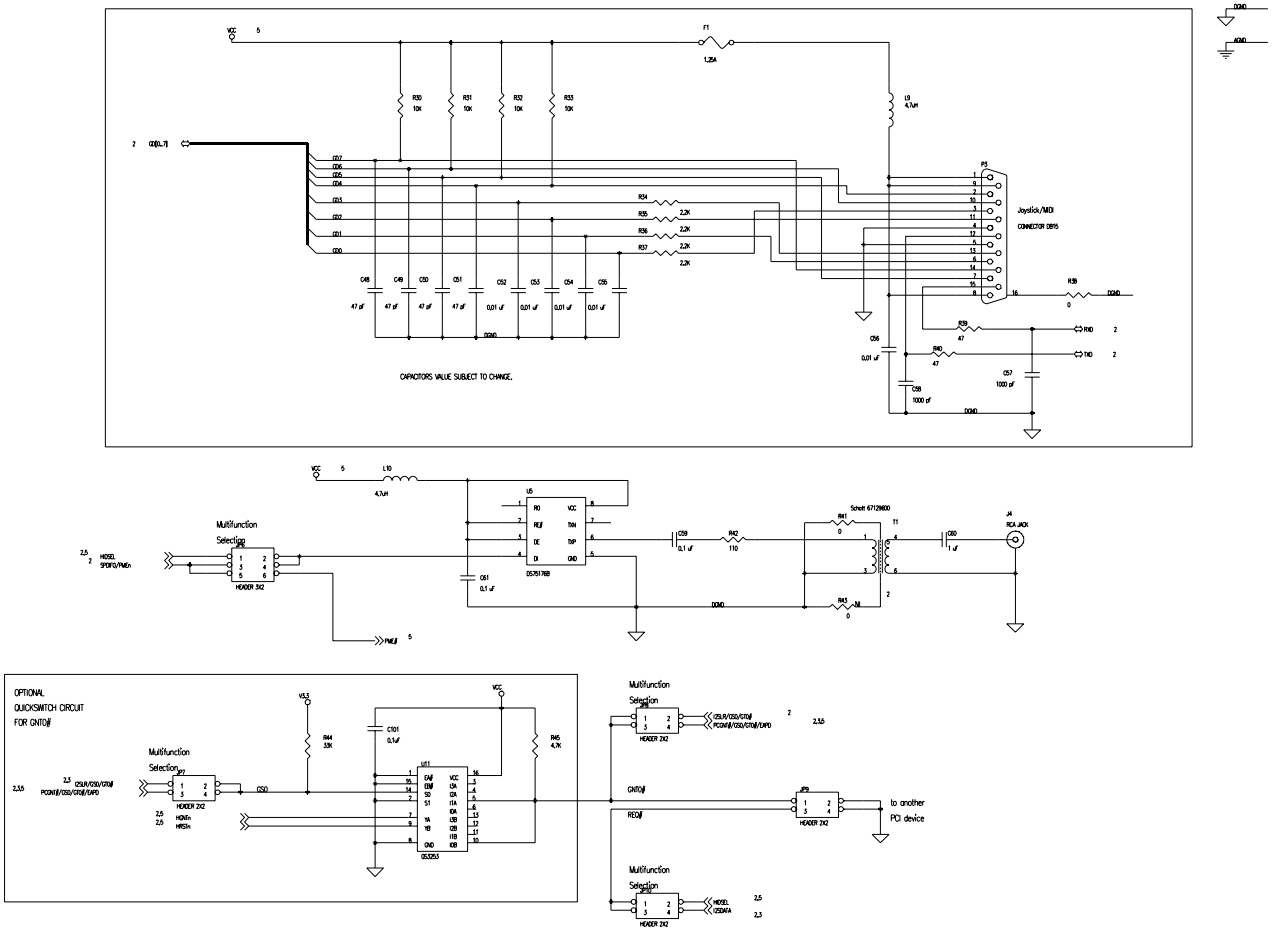
Figure 17 Audio Interface

Figure 18 Game Port and S/PDIF Interfaces
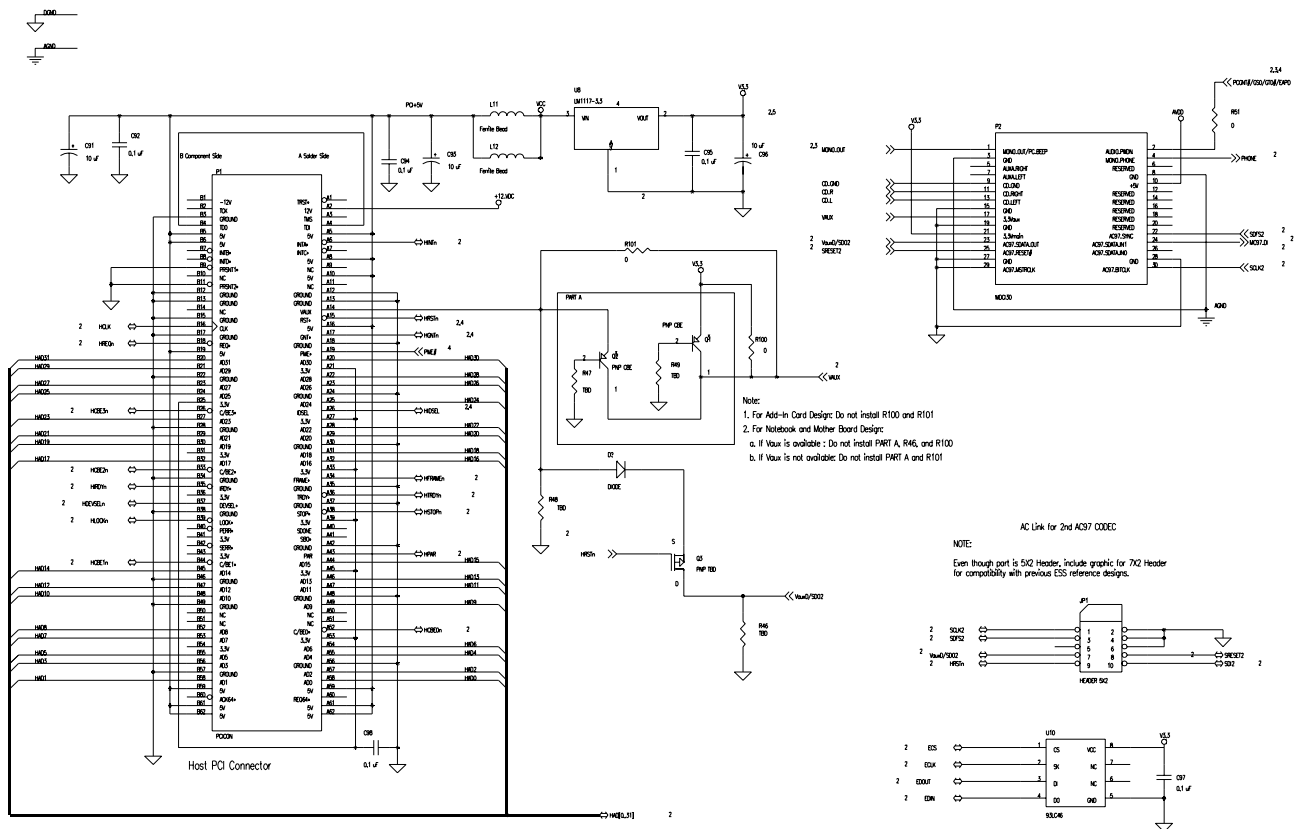
Figure 19 PCI Bus Interface

APPENDIX B: BILL OF MATERIALS

Item	Reference Designator	Qty	Component Description
1	U1	1	ES1988, 100 pin TQFP
2	U2	1	MC78M05(DPACK)
3	U3	1	LMV358M,SO8, Low Power Dual Op Amp
4	U4	1	LM4880M, Stereo Audio Power Amplifier
5	U5	1	DS75176B, Transceivers
6	U8	1	LM1117-3.3
7	U10	1	93LC46, 1K Serial EEPROM
8	R1, R13	2	Res, 5%, 1M, SMD, 0805
9	R2, R15, R16, R30, R31, R32, R33, R41, R44, R60, R117	11	Res, 5%, 10K, SMD, 0805
10	R3, R4, R22, R29, R38, R48, R49, R50, R104, R105, R110	11	Res, 5%, 0, SMD, 0805
11	R5, R6, R8, R9, R17, R19, R20, R21	8	Res, 5%, 6.8K, SMD, 0805
12	R10	1	Res, 5%, 33K, SMD, 0805
13	R11	1	Res, 5%, 22K, SMD, 0805
14	R12, R34, R35, R36, R37	5	Res, 5%, 2.2K, SMD, 0805
15	R18	1	Res, 5%, 51K, SMD, 0805
16	R23, R28	2	Res, 1%, 27K, SMD, 0805
17	R24, R25	2	Res, 1%, 20K, SMD, 0805
18	R39, R40	2	Res, 5%, 47, SMD, 0805
19	R42	1	Res, 5%, 75, SMD, 0805
20	R46	1	Res, 5%, 3.3K, SMD, 0805
21	R27, R102	2	Res, 5%,100K,SMD,0805
22	R99	1	Res, 5%,220K,SMD,0805
23	C1	1	Cap, Cera, SMD, 5%, 50V, 10pF, 0805
24	C3, C7, C11, C12, C13, C18, C19, C46, C63, C91, C93, C96	12	Cap, Radial 20%,25V, 10uF, Size .100"
25	C5, C6, C8, C9, C14, C16, C17, C26, C27, C45, C59, C61, C62, C92, C94, C95, C97, C98	18	Cap, Cera, SMD, 10%, 50V, 0.1uF, 0805
26	C10, C15, C57, C58	4	Cap, Cera, SMD, 10%, 50V, 1000pF, 0805
27	C20, C21, C52, C53, C54, C55, C56	7	Cap, Cera, SMD, 10%, 50V, 0.01uF, 0805
28	C22, C23, C24, C25, C28, C29, C30, C31, C32, C35, C36, C39, C41, C60	14	Cap, Cera, SMD, 10%, 50V, 1uF, 0805
29	C33	1	Cap, Cera, SMD, 5%, 50V, 180pF, 0805
30	C34	1	Cap, Cera, SMD, 5%, 50V, 0.33uF, 0805
31	C38, C44	2	Cap, Cera, SMD, 5%, 50V, 330pF, 0805
32	C37, C47	2	Cap, Cera, SMD, 5%, 50V, 5pF, 0805
33	C40, C42	2	Cap, Radial 20%,25V, 100uF, Size .100"
34	C43	1	Cap, Radial 20%,25V, 3.3uF, Size .100"
35	C48, C49, C50, C51	4	Cap, Cera, SMD, 10%, 50V, 47pF, 0805
36	C2	1	Cap, Cera, SMD, 5%, 50V, 33pF, 0805
37	C4	1	Cap, Cera, SMD, 5%, 50V, 1500pF, 0805

Item	Reference Designator	Qty	Component Description
38	L1	1	Inductor, 1.0uH, 1206
39	L2, L6, L9, L10, L11, L12	6	HighCurrentBead, CTC (HH-1H3216-500), 1206
40	L3, L4, L5, L7, L8	5	Ferrite Bead, TDK (CB30 – 0805), 0805
41	Q2	1	2N7002LT1
42	F1	1	Fuse, 1.25A, Thru-hole
43	Y1	1	Xtal, 49.152MHz, 3rd Overtone, 50ppm, HC-49/U
44	T1	1	SCHOTT-67129600, Transformer, Thru-hole
45	P1, P2	2	AMP 3-179397-0
46	P3	1	DB15 female connector (right angle)
47	J1, J2, J3	3	Stereo jack connector, 5 pin, SJ372N
48	J4	1	RCA JACK
49	J5, J7	2	2mm Wafer Socket, 4 pin
50	J6, JP1	2	HEADER 2X1
51	JP2	1	HEADER 3X1
52	J8	1	HEADER 4X1
53	JP7	1	HEADER 3X2
54	JP3	1	HEADER 10X2
55		1	Bracket

ORDERING INFORMATION

Part Number	Package
ES1988S	100-pin TQFP

ESS Technology, Inc.
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Fremont, CA 94538
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