The ATM Forum

Technical Committee

ATM on Fractional E1/T1

AF-PHY-0130.00

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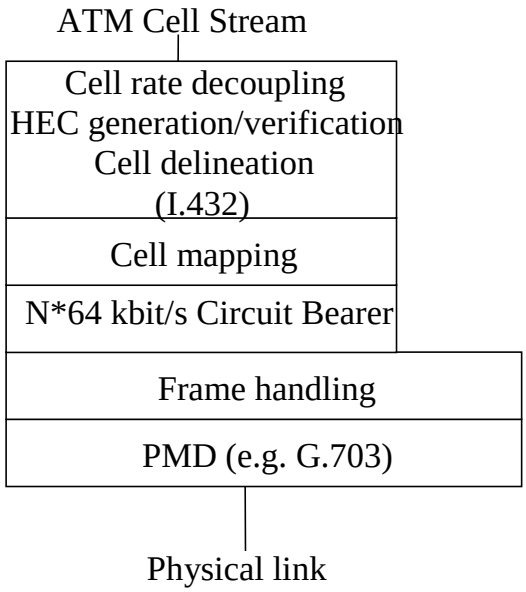
1. Introduction.

This document specifies the requirements for the ATM Forum on how to map ATM on a "circuit-mode connection" supporting unrestricted information transfer rates at integer multiples of 64 kbit/s up to the maximum rate of the interface (ref: ITU-T rec. I.231.10 [1]). The physical interface may typically be DS1 or E1 (or any other physical interface). The specification shall apply for any N*64 kbit/s rate up to 1920 kbit/s (N=30) and be independent of type of interface (UNI or NNI).

Figure 1 shows the physical layer functionality of ATM when mapped on a circuit bearer.

Figure 1 Physical Layer Functions for transfer rates at integer multiples of 64 kbit/s.



Observe that the mechanism for how to map ATM on a circuit bearer is not different from the general mechanism described in earlier specifications, e.g. in af-phy-0064.000 [2], “E1 Physical Interface Specification” and in G.804, [3] “ATM Cell Mapping into Plesiochronous Digital Hierarchy”.

2. Acronyms

HEC	Header Error Control
ISDN	Integrated Services Digital Network
ITU-T	International Telecommunication Union - Telecommunication
NNI	Network-Node Interface
PMD	Physical Medium Dependent
TC	Transmission Convergence

UNI User Network Interface

3. Physical Medium Dependent (PMD) Sublayer

Will not be defined in this specification.

The content of this specification is independent of the PMD sublayer.

4. N*64 kbit/s Circuit Sublayer

4.1 Transport Specific TC Functions

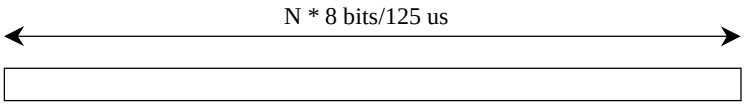
4.1.1 N*64 kbit/s Circuit Bearer Transmission Frame Format

The N*64 kbit/s circuit bearer transmission frame format specified here is compliant to the ISDN "Circuit-mode Multiple-rate Unrestricted 8 kHz Structured Bearer Service Category (ref: ITU-T rec. I.231.10 [1]). The N*64 kbit/s circuit bearer for ATM allows only point-to-point configurations.

(R1) The assignment of the N 64 kbit/s time slots shall support both contiguous and non-contiguous configuration. The assignment has only local meaning. In particular, the contiguous assignment at one interface does not mean that the time slots are assigned contiguously within the network or at the terminating interface.

(R2) The N*64 kbit/s Circuit Bearer shall support octet alignment of an unrestricted octet stream supporting sequence integrity. The transmission frame shall consist of N time slots (octets). The frame repetition rate is 8000 Hz. All timeslots of the N*64 kbit/s Circuit Bearer shall be available for carrying data traffic. The frame is shown in Figure 2.

Figure 2 N*64 kbit/s Circuit Bearer Frame Structure



(R3) The N*64 kbit/s time slots selected shall belong to a single physical interface

(R4) The number of assigned time slots is symmetrical.

(R5) The N*64 kbit/s circuit bearer shall support assignment of all those time slots, which are meant for user data traffic in the physical interface specifications. (E.g. TS0 and TS16 at the E1 interface are by default reserved and not available for circuit bearer)

4.1.2 Frame Handling

(R6) Framing shall be provided by the physical layer as a primitive.

4.2 ATM-Specific TC Functions

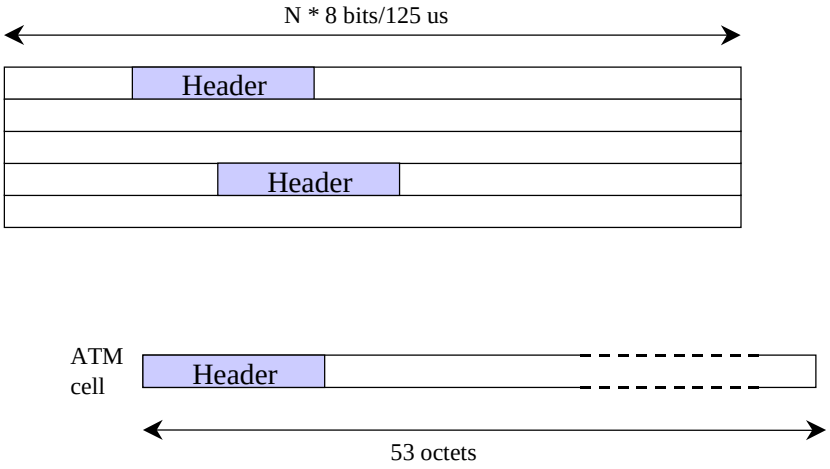
4.2.1 ATM Cell Mapping

(R7) The ATM cell is mapped into all bits of the N*64 kbit/s Circuit Bearer frame as shown in Figure 3. The ATM cell octet structure shall be aligned with the octet structure of the frame.

(R8) There shall be no relationship between the beginning of an ATM cell and the beginning of an N*64 kbit/s Circuit Bearer frame.

Note: Since the frame payload capacity (N octets) is not an integer multiple of cell length (53 octets), ATM cells will cross the N*64 kbit/s Circuit Bearer frame boundary.

Figure 3 N*64 kbit/s Circuit Bearer Frame Structure Used to Transport ATM Cells.



4.2.2 Cell Rate Decoupling

(R9) The cell rate adaptation to the payload capacity of the N*64 kbit/s Circuit Bearer frame (N*64 kbit/s) shall be performed by the insertion of idle cells as defined in ITU-T Recommendation I.432.1 [4], Section 7.3.5. The header (and payload) pattern for idle cells shall be as defined in [4], Table3/I.432.1.

4.2.3 Header Error Control (HEC) Processing

(R10) The Header Error Control (HEC) value shall be verified as specified by ITU-T Recommendation I.432.1 [4], Section 7.3.2.1.

(O1) When single bit HEC errors are corrected, this shall be done as specified by ITU-T Recommendation I.432.1 [4], Section 7.3.2.1.

(R11) The Header Error Control (HEC) value shall be generated in compliance with ITU-T Recommendation I.432.1 [4], Section 7.3.2.2.

4.2.4 Cell Delineation and Scrambling

(R12) The cell delineation function shall be performed using the HEC mechanism as defined in ITU-T Recommendation I.432.1 [4], Section 7.3.3.

(R13) The ATM cell payload shall be scrambled using a self-synchronizing scrambler with polynomial $x^{43} + 1$as defined in ITU-T Recommendation I.432.1 [4], Section 7.3.4.1.

5. References

[1] ITU-T Recommendation I.231.10 on "Circuit-mode Multiple-rate Unrestricted 8 kHz Structured Bearer Service Category", August 1992.
[2] ATM Forum af-phy-0064.000, E1 Physical Interface Specification, September 1996.
[3] ITU-T Recommendation G.804, ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH), July 1995.
[4] ITU-T Recommendation I.432.1 on B-ISDN user-network interface – Physical layer specification: General characteristics, February 1999.